

Design of New Cascaded Multilevel Inverter with Symmetrical DC-voltage Source

Maham Fatima^{1*}, Umer Shahid¹, Abubakar Siddique², Waseem Aslam²

¹ Department of Electrical Engineering, University of Engineering and Technology, Lahore, Pakistan 54890.

² School of Electrical & Electronics Engineering, North China Electric Power University, 102206, Beijing, China.

* Corresponding author. Email: mahamfatima148@gmail.com

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Abstract: In this paper, a new cascaded module of multilevel inverter is proposed. The proposed topology produces a large number of levels with reduced total harmonic distortion (THD). This module consists of less number of MOSFETs and gate drivers which optimize the design of MLI in term of complexity, cost, control and installation. The performance analysis of proposed module is done by using a modulation technique. Simulation results for 17-level are evaluated on MATLAB/SIMULINK.

Key words: Multilevel inverter, symmetrical DC source, innovative PWM, THD.

1. Introduction

Renewable energy resource (RES) has become more attractive and fascinating due to the advancement of technology. RES like solar energy, wind energy, biomass, hydropower and geothermal etc are attractive in meeting the demands of consumer than the conventional sources. By economic point of view these RESs are contributing much well due to priceless quality of solar energy. The implementation of RESs in hybrid system gives rise a tremendous regime in the domain of energy [1]. The collective advantage of maximum efficiency and minimum losses is achieved by photovoltaic, wind turbine and fuel cell. Power electronic devices MLI, converter, chopper etc play an important role with the collaboration of these RESs and distributed grid system. The concept of optimization of micro grids with distributed system is a good opportunity in gaining flexibility, reliability, control mechanism and efficient quality of power [2].

DC to AC power conversion is a key technology in the modern set-up of generation, transmission, distribution, and utilization of electric power. With the advent of recent power electronics devices, digital controllers, and sensors, the role of power inverters is also envisaged and acknowledged in frontiers such as futuristic smart grids and greater penetration of renewable energy sources-based power generation [3]. Conventional two level inverters have been used. However, these inverters give pulsating waveforms of current and voltage at their outputs and filters are needed to get fundamental frequency sinusoidal waveforms. Efficiency of this process is low since energy contained in the higher order harmonics is wasted. Keeping in view the disadvantages of conventional two level inverters, it is important to devise new inversion methodologies.

In past few decades, the concept of MLI has become more popular due to usage of RES and their demand is increasing day by day in the field of HVDC power transmission, AC motor drive, STATCOM, static var compensation, traction, pumps, PV grid tied systems, active filters, hybrid electric vehicles, flexible AC

transmission systems and integration with RES [4], [5]. The advantage of MLI is listed below [6]:

- The output of MLI will give a staircase waveform that is close to sine wave.
- Switching frequency must be low enough to get low switching losses.
- They can draw current without disturbing the source.
- They can operate at high and low frequency but low frequency gives minimum losses.

2. Literature Review

MLI is a type of power electronics device which produces large number of levels from single or multiple DC sources at the input terminal [7]. The DC source provided at the input of MLI is obtained from different sources such as PV fuel, capacitor, dc batteries etc [8]. MLI consists of semiconductor switches like MOSFET, IGBTs, BJTs and gate drivers etc. The main purpose of MLIs is to obtain a output waveform which is closely related to reference sine wave.

MLI are categorizing in the literature. The three significant MLIs are Neural point diode clamp (NPC) [9], [10], Flying Capacitor (FC) [10], [11] and Cascaded H-Bridge (CHB) [10]. They all are classified on the basis of alignment of electrical module (diode, capacitor, power switches and gate driver). The operating properties of all three types of inverter are same while each type has its own respective advantage of flexibility, ability of high power and minimum cost. Block diagram of three basic topologies is shown in Fig 1.

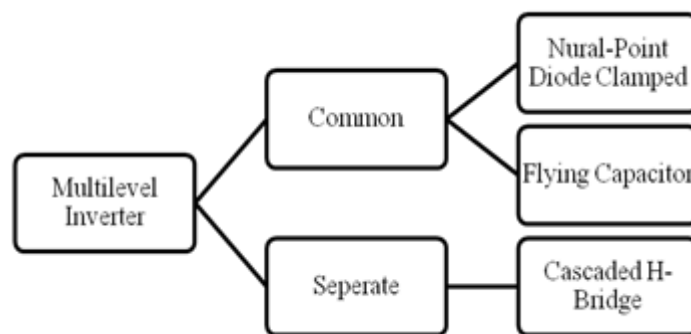


Fig. 1. Block diagram of three fundamental topologies.

The structure of NPC contains a diode by which output voltage level is adjusted. NPC operate at fundamental frequency which will make inverter efficient. Various types of NPC inverter like T-type and A-type are proposed in [9]. The presence of diode makes the circuit complex because when we switch from low to high level then the number of diodes also increases. Control of real power in single module of multi MLI become difficult [12].

Similarly, design of FC contains a capacitor. The presence of capacitor is beneficial in comparison with NPC because it can regulate the imbalance voltages. The control of real and reactive power is easy and content of harmonics is also low with respect to NPC. Beside this, some disadvantages also present in FC like switching frequency and losses are quite high due to capacitor [12]. Due to the disadvantages of both modules, Nabae proposed a first cascaded three level MLI by using two classical inverter in series connection [13]. The cascaded module has supreme importance than other topologies due to excellent nature of output waveform and high levels. But this cascaded module requires a large number of components making the circuit complex and costly. Therefore, this cascaded module was being reform by the researchers and its modified form is called as CHB [4], [11], [14].

This CHB contain a number of IGBTs, gate driver and other power switches depending upon the output

levels. Another five level inverter is proposed in [12]. In this circuit, two level inverter is used along with conventional NPC. This circuit is quite reliable in four pole induction machine derive. But the circuit moves towards complexity due to presence of two module inverter. In [11], a new topology of MLI is proposed. It is based on combination of several group of MLIs. It contains n- number of DC sources and power switches. The structure of this inverter contains more number of semiconductor switches to produce a particular level. In [15], medium voltage inverter using NPC and FC are proposed. But for the production of large levels it requires large number of components. For example, for 3-level NPC, it contain 12 switches, 2 dc sources, 6 diode, 2 capacitors while for 4-level FC, it contain 18 switches, 1 dc sources,6 capacitors.

The content of odd harmonics in the behavioral analysis of the MLI is most responsible factor for the distorted staircase waveform. To reduce the THD of MLI, number of controlling techniques are proposed in [16]-[18]. In [19], switching frequency is used as a control mechanism for the symmetrical configuration of inverter. It comprises on number of power switches, DC source and gate driver and the THD of this 15-level MLI is 10.26. In [2], pulse width modulation (PWM) is proposed. PWM is classified in level shifted and phase shifted technique. In level shifted, power is not equally distributed whereas in phase shifted, power is equally allocated in all circuits. A multicarrier PWM technique is used in [20] for the reduction of harmonics and THD but this topology is not suitable for closed-loop system. A SHE is implemented on E-Type MLI in [21]. All these techniques are used to reduce the THD and switching losses. But these techniques require algorithms which are difficult to implement.

3. Proposed Topology

The circuit proposed in this paper consists of minimum number of power switches and voltage sources. Proposed circuit is shown in Fig. 2. Cascaded module of proposed MLI consists of two modules. Each module contains nine switches, one voltage source, two diodes and two capacitors. In this way, total of eighteen switches and two voltage sources with capacitor and diode. Proposed circuit has seventeen output levels: $\pm 4V$, $\pm 7V/2$, $\pm 3V$, $\pm 5V/2$, $\pm 3V/2$, $\pm V$, $\pm V/2$ and 0. This proposed circuit is compared with other topologies in term of modulation techniques and components to analyze the behavior and THD of proposed MLI.

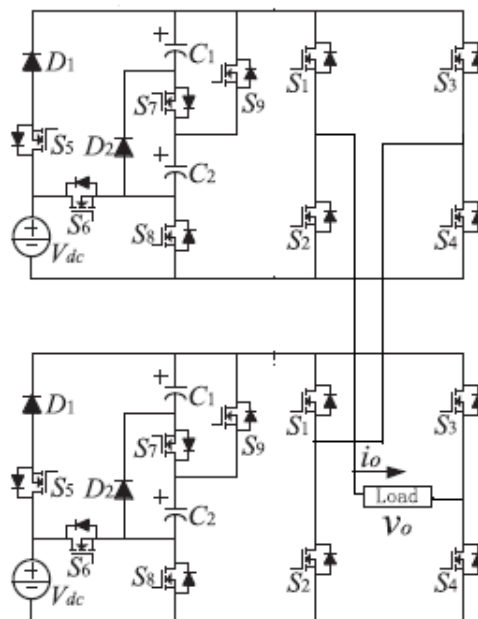


Fig. 2. Proposed cascaded module.

At $\pm 4V$, $\pm 7V/2$, $\pm 3V$ and $\pm V$, capacitors of both cascaded module discharge. At $\pm 2V$, all four capacitors are charged. At $\pm 5V/2$ and $\pm 3V/2$, two capacitors charge and remaining two capacitors discharge. At $\pm V/2$, and $\pm V$, two capacitors discharge and remaining two capacitor neither charge nor discharge. At 0, voltages become balanced. ON and OFF states of capacitor and diodes are shown in Table 1.

Table 1. States of Capacitors and Diodes

Levels	Module 1				Module 2			
	C1	C2	D1	D2	C1	C2	D1	D2
$\pm 4V$	D	D	R	R	D	D	R	R
$\pm 7V/2$	D	D	R	F	D	D	R	F
$\pm 3V$	D	D	R	F	D	D	R	F
$\pm 5V/2$	C	C	F	R	D	D	R	F
$\pm 2V$	C	C	F	R	C	C	F	R
$\pm 3V/2$	D	D	F	R	C	C	R	F
$\pm V$	D	D	R	F	D	D	R	F
$\pm V/2$	D	D	R	F	--	--	R	R
0	--	--	R	R	--	--	R	R

Here symbols D and C in the capacitors column shows discharging and charging of capacitor respectively and F and R in the diode column shows forward and reverse bias of diode respectively. Symbol -- shows capacitor charge, discharge and uncharged respectively. Current path for level (4V) and (0) is shown in Fig. 3 and Fig. 4 respectively.

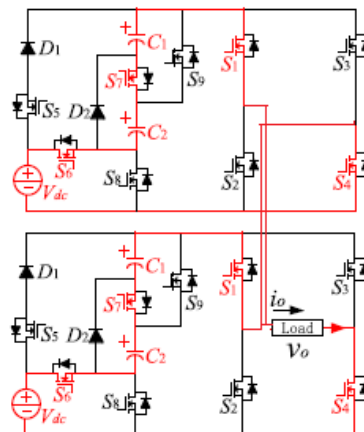


Fig. 3. Current path at 4V.

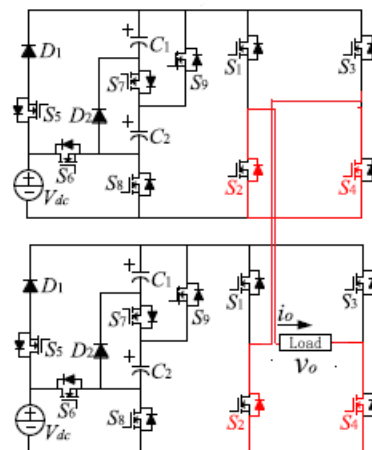


Fig. 4. Current path at 0V.

Switching states of proposed MLI are given in Table 2. Number of levels is increase by suitable combination of switching states. Sequential order of these conduction states decides that which switch is ON and OFF respectively to produce a particular level. The relation between voltage sources in symmetrical topology is given by

$$V1 = V2 \tag{1}$$

The range of output voltage level with a step of $V_{dc}/2$ is

$$+2V1 + 2V2 \text{ to } -2V1 - 2V2 \tag{2}$$

Table 2. Switching States of Proposed Circuit

Level s	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9	S1 0	S1 1	S1 2	S1 3	S1 4	S1 5	S1 6	S1 7	S1 8
4V	1	0	0	1	1	1	1	0	0	1	0	0	1	1	1	1	0	0
7V/2	1	0	0	1	1	1	0	0	1	1	0	0	1	1	1	1	0	0
3V	1	0	0	1	1	1	0	0	1	1	0	0	1	1	1	0	0	1
5V/2	1	0	0	1	1	0	0	1	0	1	0	0	1	1	1	0	0	1
2V	1	0	0	1	1	0	0	1	0	1	0	0	1	1	0	0	1	0
3V/2	1	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	1	1
V	1	0	0	1	0	0	0	1	1	1	0	0	1	0	0	0	1	1
V/2	1	0	0	1	0	0	0	1	1	0	1	0	1	0	0	0	1	1
0	0	1	0	1	0	0	0	1	1	0	1	0	1	0	0	0	1	1
-V/2	0	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0	1	1
-V	0	1	1	0	0	0	0	1	1	0	1	1	0	0	0	0	1	1
-3V/2	0	1	1	0	1	0	0	1	0	0	1	1	0	0	0	0	1	1
-2V	0	1	1	0	1	0	0	1	0	0	1	1	0	1	0	0	1	0
-5V/2	0	1	1	0	1	0	0	1	0	0	1	1	0	1	1	0	0	1
-3V	0	1	1	0	1	1	0	0	1	0	1	1	0	1	1	0	0	1
-7V/2	0	1	1	0	1	1	0	0	1	0	1	1	0	1	1	1	0	0
-4V	0	1	1	0	1	1	1	0	0	0	1	1	0	1	1	1	0	0

4. Modulation Techniques

Many techniques are briefly described in the literature for the control mechanism of MLI. For the proposed MLI, two types of techniques are employed.

- ANDED PWM
- Innovative PWM

4.1. ANDED PWM

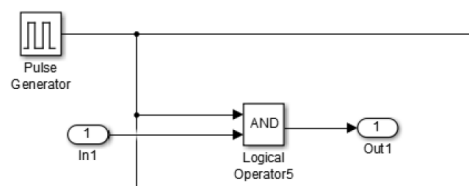


Fig. 5. Implementation of ANDED PWM.

ANDED PWM is implemented by generating a signal from pulse generator. This signal is compared with the pulse of proposed MLI and fed with AND operator to get the output. SIMULINK model for ANDED PWM is shown in Fig. 5. As the implementation of this technique in SIMULINK is easy, but the THD of MLI become too much high in comparison with the simple MLI. In order to reduce the THD, low pass filter is fed with MLI. But the presence of filter makes the MLI costly.

4.2. Innovative PWM

In innovative PWM technique, pulses of proposed MLI are sampled at low frequency. Numbers of levels are repeated several times to make the staircase waveform close to sine wave. The output is stored in an array and compared with sine wave to make sure that the output waveform of proposed MLI is close to sine wave. There is no need of filter in this technique. In this way, this topology is most suitable in reducing the THD. This technique is reliable in term of cost, low THD, minimum number of switches and ease of implementation.

5. Switching Losses

Switching losses are the losses which dissipate due to ON and OFF state of switch. Switching losses are calculated by equation given below

$$P(t) = v(t) \times i(t) \tag{3}$$

where

$$V(t) = V_{dc} - (V_{dc} V_{on}) \times (t/t_{c(on)}) \tag{4}$$

$$i(t) = I_{dc} \times (t/t_{c(on)}) \tag{5}$$

But (3) is only valid for diode clamped MLI. Switching losses in proposed MLI are caused by the charging and discharging of capacitor. So the switching losses are calculated by

$$P_s = f_s C V_b \tag{6}$$

where f_s = switching frequency, C = capacitance of capacitor and V_b = max. block voltage of each switch. The values of these parameters are listed in Table 3. By putting the values in eq (6), the total switch loss for the proposed MLI is given by

$$P_s = 26.3 f_0 C V_d^2 \tag{7}$$

The efficiency is given as

$$\eta = \text{Output} / \text{Input} \tag{8}$$

So, the theoretical efficiency of proposed MLI is given as

$$\eta = P_0 / P_s + P_0 \tag{9}$$

P_0 = output power of proposed MLI.

Table 3. Operational Parameters of Each Switch

	Switches	S1	S2	S3	S4
Module 1	f_s	f_0	f_0	$2f_0$	$2f_0$
	V_b	$0.5V_d$	$0.6V_d$	$0.5V_d$	$0.6V_d$
Module 2	f_s	$2f_0$	$2f_0$	$2f_0$	$2f_0$
	V_b	$0.5V_d$	$0.6V_d$	$0.5V_d$	$0.6V_d$
	S5	S6	S7	S8	S9
Module 1	$4f_0$	$4f_0$	$4f_0$	$4f_0$	$12f_0$

	$0.8V_d$	$0.4V_d$	$0.1V_d$	$0.7V_d$	$0.7V_d$
Module 2	$4f_0$	$4f_0$	$4f_0$	$4f_0$	$12f_0$
	$0.7V_d$	$0.5V_d$	$0.3V_d$	$0.5V_d$	$0.7V_d$

The values of component parameters are given in Table 4.

Table 4. Parameters of Proposed MLI

Names	Values
Forward Voltage drop of diode	0.3V
On state resistance of switch	4.8mΩ
Capacitance of capacitor	1000μF
I/P Dc Source	110V
O/P frequency	50Hz

6. Simulation Results

Cascaded module of proposed MLI is simulated by software MATLAB. In this section, results of proposed module and technique applied on it will display. Fig. 6 shows 17-level output, Fig. 7 shows output with ANDED PWM, Fig. 8 shows Output with filter, Fig. 9 shows output with INNOVATIVE PWM and Fig. 10-13 shows the FFT analysis and THD of all respective output. Symmetrical combination of DC source gives a 17-Level. This module is tested under ANDED PWM and Innovative PWM.

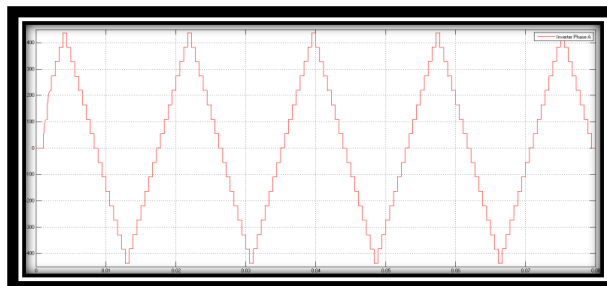


Fig. 6. Single phase 17-level output waveform.

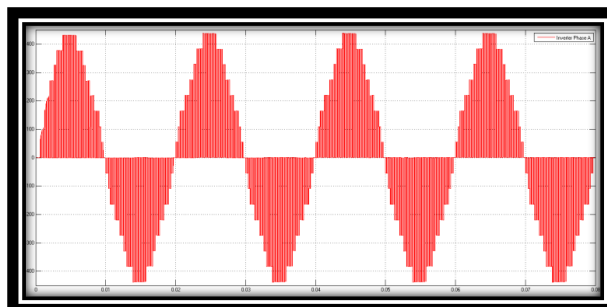


Fig. 7. 17-Level output waveform with ANDED PWM.

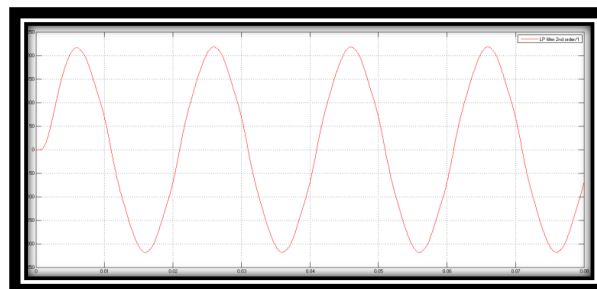


Fig. 8. Output waveform with ANDED PWM & filter.

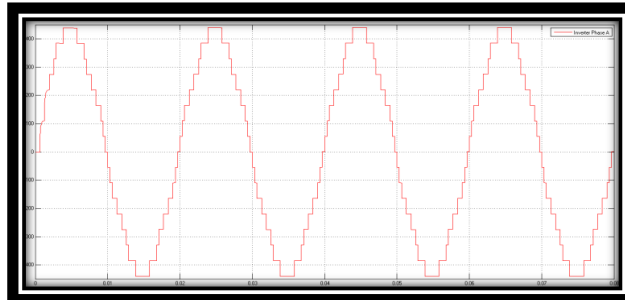


Fig. 9. 17-Level output waveform with innovative PWM.

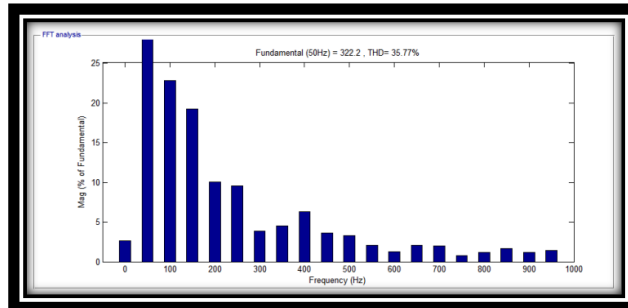


Fig. 10. FFT analysis of 17-level.

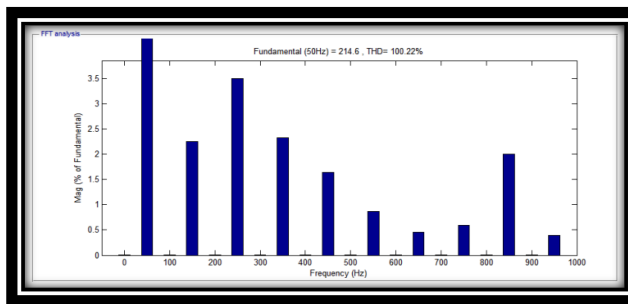


Fig. 11. FFT analysis of 17-level with ANDED PWM.

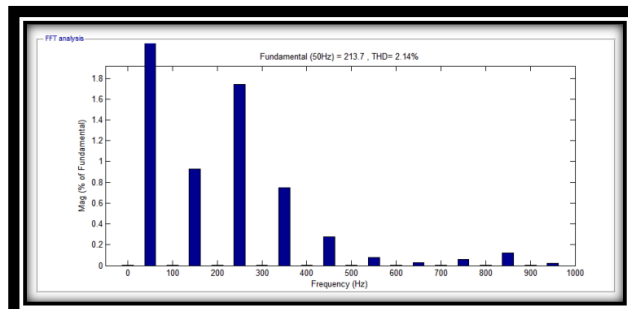


Fig. 12. FFT analysis of 17-level with ANDED PWM & filter.

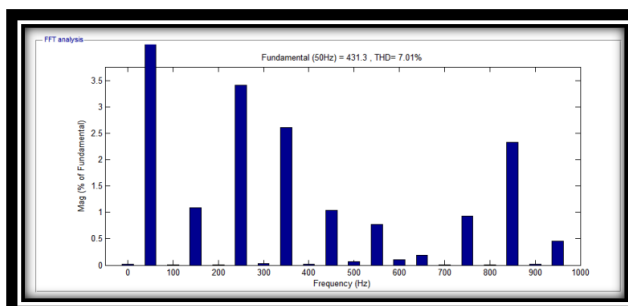


Fig. 13. FFT analysis of 17-level with innovative PWM.

7. Comparison

Comparison of proposed MLI is done with the inverter in [21], [22] in term of number of components. The comparison of components is listed in Table 5. As it is clear from the table, that the minimum number of components for proposed MLI requires less area of installation as compared with other inverters.

Table 5. Comparison Paramters

Parameter	Proposed MLI	MLI in [21]	MLI in [22]
N_{source}	2	8	6
$N_{\text{capacitor}}$	4	0	0
N_{switch}	18	32	18
N_{diode}	4	0	8

Here N_{source} , $N_{\text{capacitor}}$, N_{switch} and N_{diode} represent the number of sources, capacitors, switches and diodes. Comparison of proposed MLI with modulating techniques is listed in Table 6.

Table 6. Comparison with Modulation Techniques

MODULATION TECHNIQUE	THD %
SIMPLE	35
ANDED PWM	100
FILTER	2.14
Innovative PWM	7

8. Conclusion

In this paper, symmetrical cascaded module of MLI is proposed. The structural configuration of this MLI contains less number of switches. This leads to the reduction in complexity of design of MLI. The performance of this MLI is examined under different modulating techniques. It has ben shown that not only number of levels increase with this proposed topology but also there is remarkable decrease in THD. There is no need of filter with innovative modulation technique. This technique is more reliable in term of cost and reliability than other techniques. Hence, the proposed topology of MLI is efficient in term of optimum strutural design and installation. It has remarkable applications in industries, AC drives, and PV modules.

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Maham Fatima was born in Bahawalpur, Pakistan. She received her bachelor degree in electrical (power) engineering from Islamia University of Bahawalpur (IUB). She did the MS in electrical engineering from University of Engineering & Technology, (UET) Lahore. Her area of research is control systems, nonlinear dynamical systems and power electronics.



Umer Shahid was born in Lahore, Pakistan in 1993. He received his BS degree in 2015 and MS degree in 2017 in electrical engineering from University of Engineering and Technology, Lahore (UET). He is currently serving as senior lecturer in University of Engineering and Technology Lahore since spring of 2016. His area of research is power electronic converters, nonlinear dynamic control systems and renewable energy systems.



Abubakar Siddique was born in Pakistan. He received the BSc & MSc degrees in electrical engineering from the Islamia University Bahawalpur (IUB), Pakistan, in 2011 and 2013 respectively. He is pursuing the PhD degree from School of Electrical & Electronics Engineering, North China Electric Power University, (NCEPU) 102206, Beijing, China. His research area is FACTS, power quality analysis, power electronics, renewable energy and transient stability.



Waseem Aslam was born in Pakistan. He received the B.S. and M.S. degrees from UCET, Islamia University of Bahawalpur, Punjab, Pakistan in 2011 and 2013, respectively, all in electrical engineering (power). Currently, he is pursuing the PhD degree at North China Electric Power University, (NCEPU) Beijing, China. He was working as an electrical engineer in a Govt. Engineering Institute. His research interests include FACTS, power quality analysis, power electronics, stability, and smart grids.