A Refined Space Vector PWM Signal Generation for Eleven-level Inverter

G.Sambasiva Rao and K.Chandra Sekhar, *Member, IEEE*

***Abstract*—A refined space vector modulation scheme for an eleven-level inverter system for dual-fed induction motor drive, using only the instantaneous sampled reference signals is presented in this paper. The dual-fed structure is realized by opening the neutral-point of the conventional squirrel cage induction motor. The eleven-level inversion is obtained by feeding the dual-fed induction motor with asymmetrical four-level inverter from one end and symmetrical three-level inverter from other end. The proposed space vector pulse width modulation technique does not require the sector information and look-up tables to select the appropriate switching vectors. The inverter leg switching times are directly obtained from the instantaneous sampled reference signal amplitudes and centers the switching times for the middle space vectors in a sampling time interval, as in the case of conventional space vector pulse width modulation.**

***Index Terms*—Dual-fed induction motor, eleven-level inverter, middle space vectors, sinusoidal reference signals, space vector PWM.**

I. Introduction

The two most widely used pulse width modulation (PWM) schemes for multilevel inverters are the carrier-based sine-triangle PWM (SPWM) scheme and the space vector PWM (SVPWM) scheme. These modulation schemes have been extensively studied and compared for the performance parameters with two level inverters [1]. The SPWM schemes are more flexible and simpler to implement, but the maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage [2]. In SVPWM schemes, a reference space vector is sampled at regular intervals to determine the inverter switching vectors and their time durations, in a sampling time interval. The SVPWM scheme gives a more fundamental voltage and better harmonic performance compared to the SPWM schemes [3]. The maximum peak of the fundamental component in the output voltage obtained with space vector modulation is 15% greater than with the sine-triangle modulation scheme. But the conventional SVPWM scheme requires sector identification and look-up tables to determine the timings for various switching vectors of the inverter, in all the sectors [4], [5] and for over-modulation, the PWM signal generation is explained in [6]-[8]. This makes the implementation of the SVPWM scheme quite complicated. It has been shown that, for two-level inverters, a SVPWM like performance can be obtained with a SPWM scheme by adding a common mode voltage of suitable magnitude, to the sinusoidal reference signals [9]. A simplified method, to determine the correct offset times for centering the time durations of the middle space vectors, in a sampling time interval, is presented [10], for the two-level inverter.

The SPWM scheme, when applied to multilevel inverters, uses a number of level-shifted carrier signals to compare with the sinusoidal reference signals [11]. The SVPWM for multilevel inverters [12], [13] involves mapping of the outer sectors to an inner subhexagon sector, to determine the switching time interval, for various space vectors. Then the switching space vectors corresponding to the actual sector are switched, for the time durations calculated from the mapped inner sectors. It is obvious that such a scheme, in multilevel inverters, will be very complex, as a large number of sectors and inverter vectors are involved. This will also considerably increase the computation time.

A modulation scheme is presented in [14], where a fixed common mode voltage is added to the reference signal throughout the modulation range. It has been shown that common mode addition will not result in a SVPWM-like performance, as it will not centre the middle space vectors in a sampling interval [15]. The common mode voltage to be added in the reference phase voltages, to achieve SVPWM-like performance, is a function of the modulation index for multilevel inverters. A SVPWM scheme based on the above principle has been presented [16], where the switching time for the inverter legs is directly determined from sampled sinusoidal reference signal amplitudes. This technique reduces the computation time considerably more than the conventional SVPWM techniques do, but it involves region identifications based on modulation indices. While this SVPWM scheme works well for a three-level PWM generation, it cannot be extended to multilevel inverters of levels higher than three, as the region identification becomes more complicated. A carrier-based PWM scheme has been presented [17], where sinusoidal references are added with a proper offset voltage before being compared with carriers, to achieve the performance of a SVPWM. The offset voltage computation is based on a modulus function depending on the DC link voltage, number of levels and the sinusoidal reference signal amplitudes. A SVPWM scheme is presented [18], where the switching time for the inverter legs is directly determined from sampled sinusoidal reference signal amplitudes for five-level inverter where two three-level inverters feed the dual-fed induction motor. A carrier based SPWM scheme is presented [19] for five-level inverter.

The objective of this paper is to present an implementation scheme for PWM signal generation for eleven-level inverter system for dual-fed induction motor, similar to the SVPWM scheme. In the proposed scheme, the dual-fed induction motor is fed with asymmetrical four-level inverter from one end and symmetrical three-level inverter from other end. The

Manuscript received July 24, 2011; revised November 16, 2011.

The authors with the Dept. of Electrical Engineering, R.V.R and J.C. College of Engineering, Guntur-522 019, INDIA (e-mail: sambasiva.gudapati@gmail.com; e-mail: cskoritala@gmail.com).

PWM switching times for the inverter legs are directly derived from the sampled amplitudes of the sinusoidal reference signals. A simple way of adding an offset voltage to the sinusoidal reference signals, to generate the SVPWM pattern, from only the sampled amplitudes of sinusoidal reference signals, is explained. The proposed SVPWM signal generation does not involve checks for region identification, as in the SVPWM scheme presented in [16]. Also, the algorithm does not require either sector identification or look-up tables for switching vector determination as are required in the conventional multilevel SVPWM schemes [12], [13]. Thus the scheme is computationally efficient when compared to conventional multilevel SVPWM schemes, making it superior for real-time implementation.

II. Eleven-Level Inverter Scheme for the Dual-Fed Induction Motor

The power circuit of the proposed drive is shown in Fig.1. An asymmetrical four-level inverter, Inverter-A and a symmetrical three-level inverter, Inverter-B feed the dual-fed induction motor. The inverter-A is composed of three conventional two-level inverters INV-1, INV-2, and INV-3 in cascade. The Inverter-B is composed of two conventional two-level inverters INV-4 and INV-5 in cascade. The DC link voltages of INV-1, INV-2, INV-3, INV-4, and INV-5 are (3/10)Edc, (3/10)Edc, (2/10)Edc, (1/10)Edc, and (1/10)Edc respectively, where Edc is the DC link voltage of an equivalent conventional single two-level inverter drive.

The leg voltage E_{A3n} of phase-A attains a voltage of (2/10)Edc if (i)The top switch S_{31} of INV-3 is turned on (Fig.1) and (ii) The bottom switch S_{24} of INV-2 is turned on. The leg voltage E_{A3n} of phase-A attains a voltage of (5/10)Edc if (i) the top switch S_{31} of INV-3 is turned on (ii) The top switch S_{21} of INV-2 is turned on and (iii)The bottom switch S_{14} of INV-1 is turned on. The leg voltage E_{A3n} of phase-A attains a voltage of (8/10)Edc if (i) the top switch S_{31} of INV-3 is turned on (ii) The top switch S_{21} of INV-2 is turned on and (iii)The top switch S_{11} of INV-1 is turned on. The leg voltage E_{A3n} of phase-A attains a voltage of zero volts if the bottom switch S_{34} of the INV-3 is turned on. Thus the leg voltage E_{A3n} attains four voltages of 0, (2/10)Edc, (5/10)Edc, and (8/10)Edc, which is basic characteristic of a 4-level inverter. Similarly the leg voltages E_{B3n} and E_{C3n} of phase-B and phase-C attain the four voltages of 0, (2/10)Edc, (5/10)Edc, and (8/10) Edc.

The leg voltage $E_{A5n'}$ of phase-A attains a voltage of (1/10)Edc if (i)The top switch S_{51} of INV-5 is turned on and (ii) The bottom switch S_{44} of INV-4 is turned on . The leg voltage $E_{A5n'}$ of phase-A attains a voltage of (2/10)Edc if (i) The top switch S_{51} of INV-5 is turned on and (ii) The top switch S_{41} of INV-4 is turned on . The leg voltage $E_{A5n'}$ of phase-A attains a voltage of zero volts if the bottom switch S_{54} of the INV-5 is turned on. Thus the leg voltage $E_{A5n'}$ attains three voltages of 0, (1/10)Edc, and (2/10)Edc, which is basic characteristic of a 3-level inverter. Similarly the leg voltages $E_{B5n'}$ and $E_{C5n'}$ of phase-B and phase-C attain the three voltages of 0, (1/10)Edc, and (2/10)Edc.

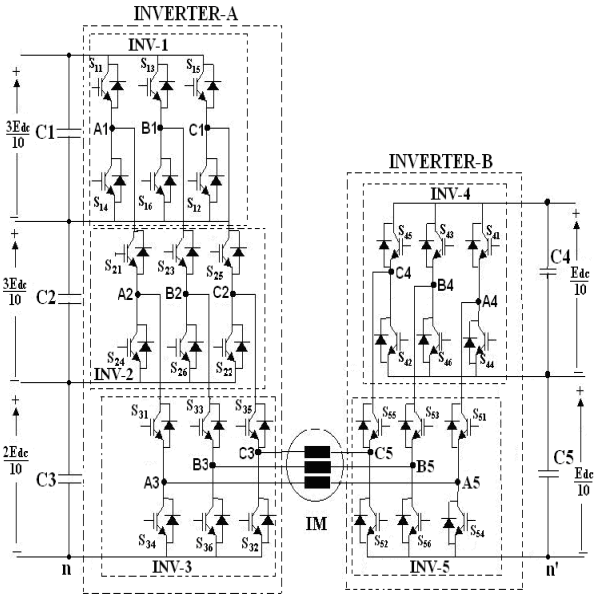

Fig. 1. Schematic circuit diagram of the proposed 11-level inverter drive scheme.

Thus, one end of dual-fed induction motor may be connected to a DC link voltage of either zero or (2/10)Edc or (5/10)Edc or (8/10)Edc and other end may be connected to a DC link voltage of either zero or (1/10)Edc or (2/10)Edc. When both the inverters, Inverter-A and Inverter-B drive the induction motor from both ends, eleven different levels are attained by each phase of the induction motor. If we assume that the points n and n' are connected, the eleven levels generated for phase-A are shown in Table I.

TABLE I: The Eleven Levels Realized in the Phase-A Winding

Leg-voltage of phase A, E_{A3n}	Leg-voltage of phase A, $E_{A5n'}$	Motor phase voltage $E_{A3A5} = E_{A3n} - E_{A5n'}$	Level
0	(2/10) Edc	-(2/10) Edc	Level 1
0	(1/10)Edc	-(1/10)Edc	Level 2
0	0	0	Level 3
(2/10) Edc	(1/10) Edc	(1/10)Edc	Level 4
(2/10) Edc	0	(2/10)Edc	Level 5
(5/10) Edc	(2/10) Edc	(3/10)Edc	Level 6
(5/10) Edc	(1/10) Edc	(4/10) Edc	Level 7
(5/10) Edc	0	(5/10) Edc	Level 8
(8/10) Edc	(2/10) Edc	(6/10) Edc	Level 9
(8/10) Edc	(1/10) Edc	(7/10) Edc	Level 10
(8/10) Edc	0	(8/10) Edc	Level 11

III. Voltage Space Vectors of Proposed Scheme

At any instant, the combined effect of 120^0 phase shifted three voltages in the three windings of the induction motor could be represented by an equivalent space vector. This space vector Es, for the proposed scheme is given by

$$Es = E_{A3A5} + E_{B3B5} . e^{j(2\pi/3)} + E_{C3C5} . e^{j(4\pi/3)}. \quad (1)$$

By substituting expressions for the equivalent phase voltages in (1),

$$Es = (E_{A3n} - E_{A5n'}) + (E_{B3n} - E_{B5n'}). e^{j(2\pi/3)} + (E_{C3n} - E_{C5n'}). e^{j(4\pi/3)} \quad (2)$$

This equivalent space vector Es can be determined by

resolving the three phase voltages along mutually perpendicular axes, d-q axes of which d-axis is along the A-phase (Fig.2). Then the space vector is given by [19]

$$Es = Es\,(d) + jEs(q) \tag{3}$$

where Es(d) is the sum of all voltage components of E_{A3A5}, E_{B3B5}, and E_{C3C5} along the d-axis and $Es(q)$ is the sum of the voltage components of E_{A3A5}, E_{B3B5}, and E_{C3C5} along the *q-axis*. The voltage components $Es(d)$ and $Es(q)$ can be thus expressed by the following transformation,

$$E_S(d) = E_{A3A5}(d) + E_{B3B5}(d) + E_{C3C5}(d) \tag{4}$$
$$E_S(q) = E_{B3B5}(q) + E_{C3C5}(q) \tag{5}$$

$$\begin{bmatrix} Es\,(d) \\ Es\,(q) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} E_{A3A5} \\ E_{B3B5} \\ E_{C3C5} \end{bmatrix} \tag{6}$$

By substituting expressions for the equivalent phase voltages in (6),

$$\begin{bmatrix} (d) \\ Es(q) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} E_{A3n} - E_{A5n'} \\ E_{B3n} - E_{B5n'} \\ E_{C3n} - E_{C5n'} \end{bmatrix} \tag{7}$$

The inverters can generate different levels of voltage vectors in the three phases of induction motor depending upon the condition of the switchings of inverter and for each of the different combinations of leg voltages, E_{A3n}, E_{B3n}, and E_{C3n} for the inverter-A and $E_{A5n'}$, $E_{B5n'}$, and $E_{C5n'}$ for the inverter-B. The different equivalent voltage space vectors can be determined using (3) and (7). The possible combinations of space vectors will occupy different locations as shown in Fig.3. There are in total 331 locations forming 600 sectors in the space vector point of view. The resultant hexagon (Fig.3) can be divided into ten layers: layer-1(innermost layer); layer-2(next outer layer) and so on.

IV. Effect of Common-Mode Voltage in Space Vector Locations

In the above analysis to generate the different levels and the space vector locations, the points n and n' are assumed to be connected. When the points n and n' are not connected (as in the proposed topology, Fig.1), the actual motor phase voltages are

$$E_{A3A5} = E_{A3n} - E_{A5n'} - E_{n'n} \tag{8}$$
$$E_{B3B5} = E_{B3n} - E_{B5n'} - E_{n'n} \tag{9}$$
$$E_{C3C5} = E_{C3n} - E_{C5n'} - E_{n'n} \tag{10}$$

$E_{n'n}$ is the common-mode voltage and is given by

$$E_{n'n} = \frac{1}{3}(E_{A3n} + E_{B3n} + E_{C3n}) - \frac{1}{3}(E_{A5n'} + E_{B5n'} + E_{C5n'}) \tag{11}$$

Substituting these expressions in (1)

$$E_S = (E_{A3n} - E_{A5n'} - E_{n'n}) + (E_{B3n} - E_{B5n'} - E_{n'n}).\, e^{j(2\pi/3)} + (E_{C3n} - E_{C5n'} - E_{n'n}).\, e^{j(4\pi/3)} = (E_{A3n} - E_{A5n'}) + (E_{B3n} - E_{B5n'}).\, e^{j(2\pi/3)} + (E_{C3n} - E_{C5n'}).\, e^{j(4\pi/3)} - (E_{n'n} + E_{n'n}.\, e^{j(2\pi/3)} + E_{n'n}.\, e^{j(4\pi/3)})$$

In this equation

$$(E_{n'n} + E_{n'n}.\, e^{j(2\pi/3)} + E_{n'n}.\, e^{j(4\pi/3)}) = E_{n'n} - \tfrac{1}{2} E_{n'n} - \tfrac{1}{2} E_{n'n} = 0$$

and the equation then reduces to

$$E_S = (E_{A3n} - E_{A5n'}) + (E_{B3n} - E_{B5n'}).\, e^{j(2\pi/3)} + (E_{C3n} - E_{C5n'}).\, e^{j(4\pi/3)}$$

This expression of Es is the same as (2), where the points n and n' are assumed to be connected. The above analysis depicts that the common-mode voltage present between the points n and n' does not effect the space vector locations. This common-mode voltage will effect only in the diversity of space vectors in different locations.

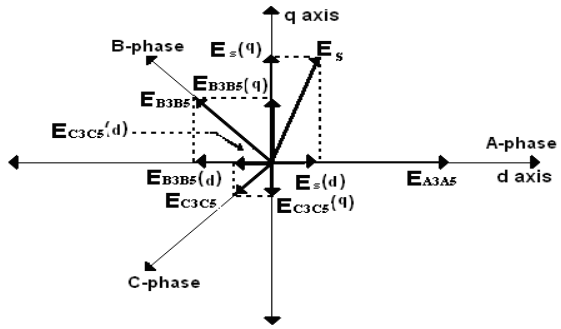

Fig. 2. Determination of equivalent space vector from phase voltages

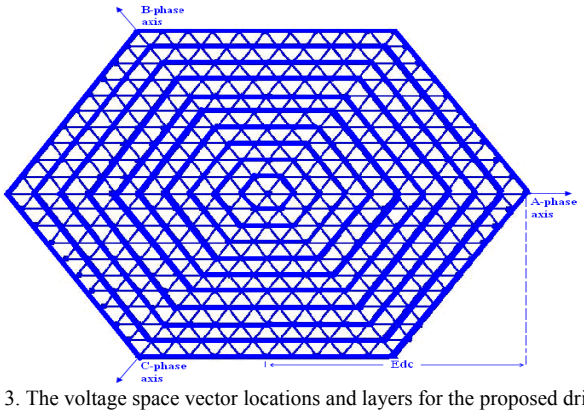

Fig. 3. The voltage space vector locations and layers for the proposed drive

V. Proposed SVPWM in Linear Modulation Range

For two-level inverters, in the SPWM scheme, each sinusoidal reference signal is compared with the triangular carrier signal and the individual phase voltages are generated [1]. To attain the maximum possible peak amplitude of the fundamental phase voltage, a common offset voltage, Eoffset1 is added to the sinusoidal reference signals [5], [14], where the magnitude of Eoffset1 is given by

$$Eoffset1 = -(Emax + Emin)/2 \tag{12}$$

where Emax and Emin are the maximum and minimum magnitudes of the three sampled sinusoidal reference signals

respectively, in a sampling time interval. The addition of this common offset voltage, Eoffset1, results in the active space vectors being centered in a sampling time interval, making the SPWM scheme equivalent to the SVPWM scheme [3]. In a sampling time interval, the sinusoidal reference signal which has lowest magnitude crosses the triangular carrier signal first, and causes the first transition in the inverter switching state. While the sinusoidal reference signal, which has the maximum magnitude, crosses the triangular carrier signal last and causes the last switching transition in the inverter switching states in a two-level SVPWM scheme [5], [15]. Thus the switching times of the active space vectors can be determined from the sampled sinusoidal reference signal amplitudes in a two-level inverter system [10].

The SPWM scheme, for eleven-level inverter, sinusoidal reference signals are compared with symmetrical level shifted ten triangular carrier signals for PWM generation [11]. After addition of offset voltage Eoffset1 to the sinusoidal reference signals, the modified sinusoidal reference signals are shown in fig.4 along with ten triangular carrier signals T1 to T10. The sinusoidal reference signals cross the triangular carrier signals at different instants in a sampling time interval Ts (Fig.4). Each time a sinusoidal reference signal crosses the triangular carrier signal, it causes a change in the inverter switching state. The changes in phase voltage and their time intervals are shown in Fig.5 in a sampling time interval Ts. The sampling time interval Ts can be split into four time intervals t_{01}, t_1, t_2, and t_{02}. The time intervals $t_{01}$and t_{02} are the time durations for the start and end inverter space vectors respectively, in a sampling time interval Ts. The time intervals t_1 and t_2 are the time durations for the middle inverter space vectors (active space vectors), in a sampling time interval Ts. It should be observed from Fig.5 that the middle space vectors are not centered in a sampling time interval Ts. Because of the level-shifted ten triangular carrier signals (Fig.4), the first crossing (termed as first_cross) of the sinusoidal reference signal cannot always be the minimum magnitude of the three sampled sinusoidal reference signals, in a sampling time interval. Similarly, the last crossing (termed as third_cross) of the sinusoidal reference signal cannot always be the maximum magnitude of the three sampled sinusoidal reference signals, in a sampling time interval. Thus the offset voltage, Eoffset1 is not sufficient to center the middle inverter space vectors, in a multilevel PWM system during a sampling time interval Ts (Fig.5). Hence an additional offset (offset2) has to be added to the sinusoidal reference signals of Fig.4, so that the middle inverter space vectors can be centered in a sampling time interval, same as a two-level SVPWM system [3]. In this paper, a simple procedure to find out the offset voltage (to be added to the sinusoidal reference signals for PWM generation) is presented, based only on the sampled amplitudes of the sinusoidal reference signals. In the proposed scheme, the sinusoidal reference signal, from the three sampled sinusoidal reference signals, which crosses the triangular carrier signal first (first_cross) and the sinusoidal reference signal which crosses the triangular carrier signal last (third_cross) are found. Once the first_cross signal and third_cross signal are known, the theory of offset calculation of (12), for the 2-level inverter, can easily be adapted for the 11-level SVPWM generation scheme.

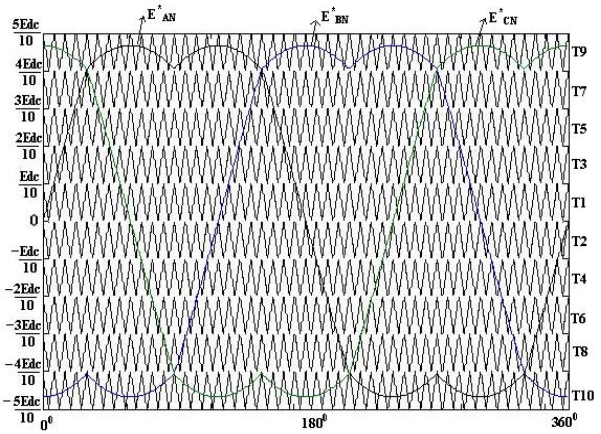

Fig. 4. Modified sinusoidal reference signals and triangular carrier signals for an eleven-level PWM scheme

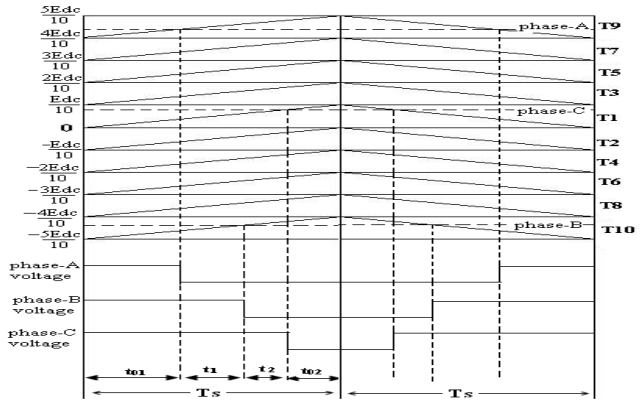

Fig. 5. Inverter switching vectors and their switching time durations during sampling time interval Ts

VI. Determination of the Offset Voltage for an Eleven-Level Inverter

Fig.4 shows modified sinusoidal reference signals and ten triangular carrier signals used for PWM generation for eleven-level inverter. The modified sinusoidal reference signals are given by

$$\begin{aligned} E^*_{AN} &= E_{AN} + Eoffset1 \\ E^*_{BN} &= E_{BN} + Eoffset1 \\ E^*_{CN} &= E_{CN} + Eoffset1 \end{aligned} \tag{13}$$

where E_{AN}, E_{BN}, and E_{CN} are the sampled amplitudes of sinusoidal reference signals during the current sampling time interval and Eoffset1 is calculated from (12). The time interval, at which the A-phase sinusoidal reference signal, E^*_{AN} crosses the triangular carrier signal, is termed as Ta-cross (Fig.6). Similarly, the time intervals, when the B-phase and C-phase sinusoidal reference signals, E^*_{BN} and E^*_{CN} cross the triangular carrier signals, are termed as Tb-cross and Tc-cross respectively. Fig.6 shows a sampling time interval when the A-phase sinusoidal reference signal is in the triangular carrier region T9 while the B-phase sinusoidal reference signal and C-phase sinusoidal reference signal are in carrier region T10 and T1 respectively. As shown in Fig.6, the time interval, Ta-cross, at which the

A-phase sinusoidal reference signal crosses the triangular carrier signal is directly proportional to the phase voltage amplitude, ($E^*_{AN} - 4Edc/10$). The time interval, Tb-cross, at which the B-phase sinusoidal reference signal crosses the triangular carrier signal, is proportional to ($E^*_{BN} + 5Edc/10$) and the time interval, Tc-cross, at which the C-phase sinusoidal reference signal crosses the triangular carrier signal, is proportional to (E^*_{CN}). Therefore

$$Ta\text{-}cross = (E^*_{AN} - 4Edc/10) \times \left(\frac{Ts}{Edc/10} \right) = T^*as - (4Ts)$$

$$Tb\text{-}cross = (E^*_{BN} + 5Edc/10) \times \left(\frac{Ts}{Edc/10} \right) = T^*bs + (5Ts)$$

$$Tc\text{-}cross = (E^*_{CN}) \times \left(\frac{Ts}{Edc/10} \right) = T^*cs \quad (14)$$

where T^*as, T^*bs and T^*cs are the time equivalents of the voltage magnitudes. The proportionality between the time equivalents and corresponding voltage magnitudes is defined as follows [8]:

$$\begin{aligned} (Edc/10)/Ts &= E^*_{AN}/T^*as \\ (Edc/10)/Ts &= E^*_{BN}/T^*bs \\ (Edc/10)/Ts &= E^*_{CN}/T^*cs \\ (Edc/10)/Ts &= Eoffset1/Toffset1 \end{aligned} \quad (15)$$

The time interval, at which the sinusoidal reference signals cross the triangular carrier signals for the first time, is termed as Tfirst_cross. Similarly, the time intervals, at which the sinusoidal reference signals cross the triangular carrier signals for the second and third time, are termed as, Tsecond_cross and Tthird_cross respectively, in a sampling time interval Ts.

$$\begin{aligned} &\text{Tfirst\_cross} = \min(\text{Ta-cross}, \text{Tb-cross}, \text{Tc-cross}) \\ &\text{Tsecond\_cross} = \text{mid}(\text{Ta-cross}, \text{Tb-cross}, \text{Tc-cross}) \\ &\text{Tthird\_cross} = \max(\text{Ta-cross}, \text{Tb-cross}, \text{Tc-cross}) \end{aligned} \quad (16)$$

The time intervals, Tfirst_cross, Tsecond_cross, and Tthird_cross, directly decide the switching times for the different inverter voltage vectors, forming a triangular sector, during one sampling time interval Ts. The time intervals for the start and end space vectors, are t_{01}= Tfirst_cross, t_{02}= (Ts − Tthird_cross), respectively (Fig.5). The middle space vectors are centered by adding a time offset, Toffset2 to Tfirst_cross, Tsecond_cross, and Tthird_cross. The time offset, Toffset2 is determined as follows. The time interval for the middle inverter space vectors, Tmiddle, is given by:

$$Tmiddle = Tthird\_cross - Tfirst\_cross \quad (17)$$

The time interval of the start and end space vector is

$$T_0 = Ts - Tmiddle \quad (18)$$

Thus the time interval of the start space vector is given by

$$T_0/2 = Tfirst\_cross + Toffset2$$

Therefore

$$Toffset2 = T_0/2 - Tfirst\_cross \quad (19)$$

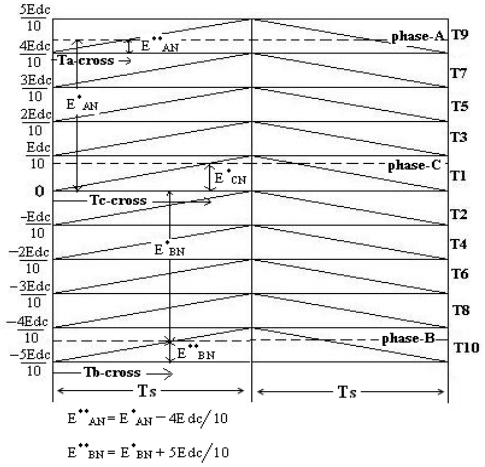

Fig. 6. Determination of the Ta-cross, Tb-cross and Tc-cross during sampling interval Ts

In this way, we can obtain offset voltages to be added for remaining samples during the time period of sinusoidal reference signal. For 11-level inverter maximum modulation index in the linear modulation range is 0.866 (the modulation index, M, is defined as the ratio of magnitude of the equivalent reference voltage space vector, generated by thethree sinusoidal reference signals, to the DC link voltage).The proposed scheme can be adapted for modulation indices lesser than 0.866. The addition of the time offset, Toffset2 to Ta-cross, Tb-cross, and Tc-cross gives the inverter leg switching times Tga, Tgb, and Tgc for phases A, B, and C respectively.

$$\begin{aligned} Tga &= Ta\text{-}cross + Toffset2 \\ Tgb &= Tb\text{-}cross + Toffset2 \\ Tgc &= Tc\text{-}cross + Toffset2 \end{aligned} \quad (20)$$

VII. Simulation Results and Discussion

The proposed SVPWM scheme is simulated using MATLAB environment with open loop E/f control for different modulation indices. The respective DC link voltages are (3/10)Edc, (3/10)Edc, (2/10)Edc, (1/10)Edc, and (1/10)Edc for the INV-1, INV-2, INV-3, INV-4, and INV-5, where Edc is the DC link voltage of an equivalent conventional single two-level inverter drive. The speed reference is translated to the frequency and voltage commands maintaining E/f. The modified three reference sinusoidal signals which are added by the total offset voltage to make SPWM scheme equivalent to the SVPWM scheme, are simultaneously compared with the triangular carrier set. A DC link voltage (Edc) of 1000 volts is assumed for simulation studies. Fig.7a shows the motor phase voltage

(E_{A3A5}) in the lowest speed range which corresponds to layer-1 operation (two-level mode) when modulation index is 0.07. Fig.7b shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM and fig.7c shows the A-phase sinusoidal reference signal after offset voltage is added. During this range of operation, motor phase current is shown in Fig.7d. Fig.8 to Fig.16 show the motor waveforms in the next speed ranges which corresponds to layer-2 operation (three-level mode) to layer-10 operation (eleven-level mode) when modulation indices are 0.15, 0.2, 0.32, 0.42, 0.5, 0.6, 0.65, 0.75, and 0.85 respectively. The ratio of triangular carrier signal frequency to reference sinusoidal signal frequency is 48 for all ranges of operation. It can be observed that the motor phase voltage and motor phase current during 11-level operation are very smooth and close to the sinusoid with lower harmonics. Fig.17 shows the decrease of percentage of total harmonic distortion (%THD) in the motor phase voltage as the number of levels increased.

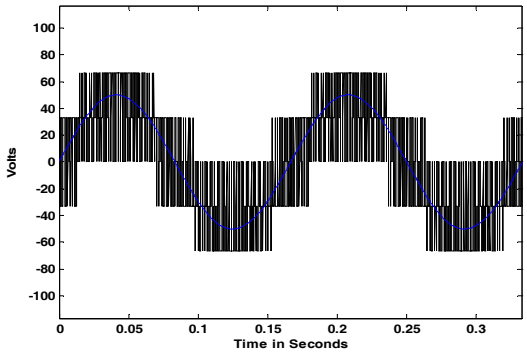

Fig. 7a. Motor phase voltage when M=0.07 (layer-1, 2-level operation)

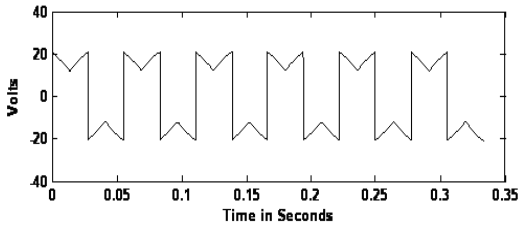

Fig. 7b. The offset voltage to be added to sinusoidal reference signals when M=0.07 (layer-1, 2-level operation)

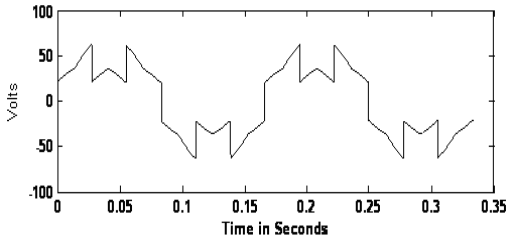

Fig. 7c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.07 (layer-1, 2-level operation)

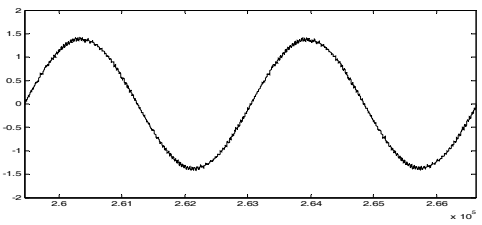

Fig. 7d. Motor phase current when M=0.07 (layer-1, 2-level operation)

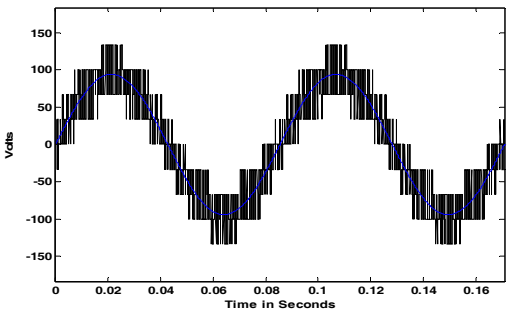

Fig. 8a. Motor phase voltage when M=0.15 (layer-2, 3-level operation)

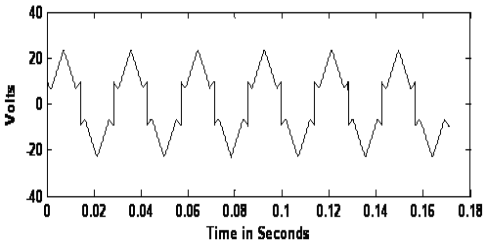

Fig. 8b. The offset voltage to be added to sinusoidal reference signals when M=0.15 (layer-2, 3-level operation)

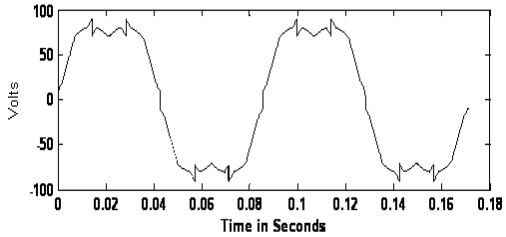

Fig. 8c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.15 (layer-2, 3-level operation)

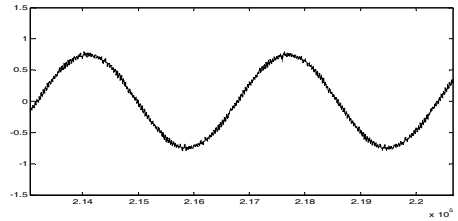

Fig. 8d. Motor phase current when M=0.15 (layer-2, 3-level operation)

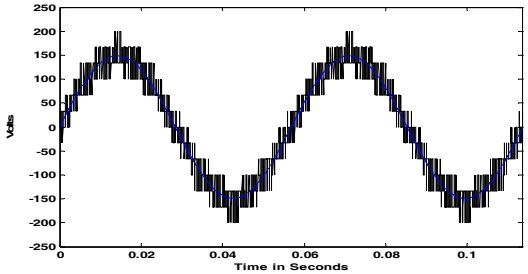

Fig. 9a. Motor phase voltage when M=0.2 (layer-3, 4-level operation)

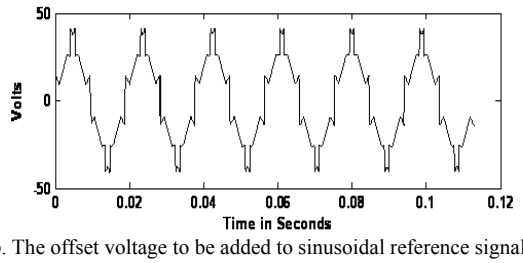

Fig. 9b. The offset voltage to be added to sinusoidal reference signals when M=0.2 (layer-3, 4-level operation)

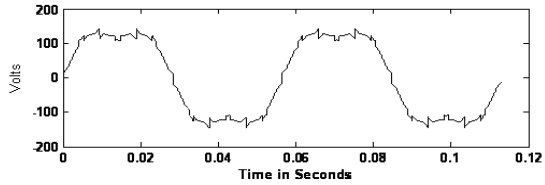

Fig. 9c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.2 (layer-3, 4-level operation)

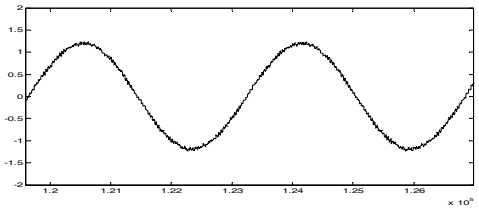

Fig. 9d. Motor phase current when M=0.2 (layer-3, 4-level operation)

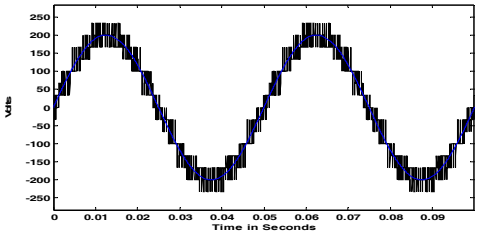

Fig. 10a. Motor phase voltage when M=0.32 (layer-4, 5-level operation)

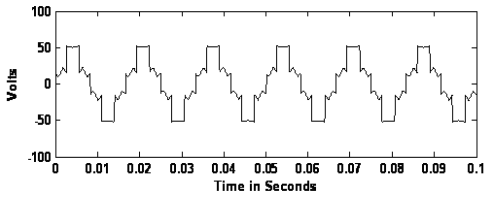

Fig. 10b. The offset voltage to be added to sinusoidal reference signals when M=0.32 (layer-4, 5-level operation)

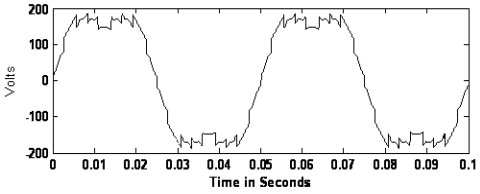

Fig. 10c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.32 (layer-4, 5-level operation)

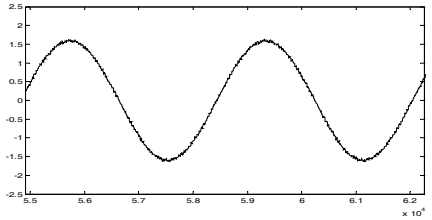

Fig. 10d. Motor phase current when M=0.32 (layer-4, 5-level operation)

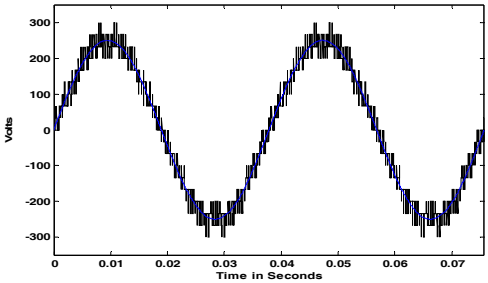

Fig. 11a. Motor phase voltage when M=0.42 (layer-5, 6-level operation)

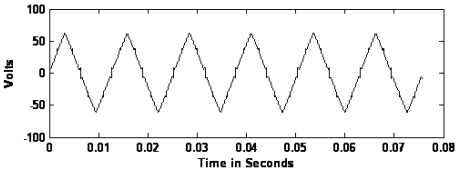

Fig. 11b. The offset voltage to be added to sinusoidal reference signals when M=0.42 (layer-5, 6-level operation)

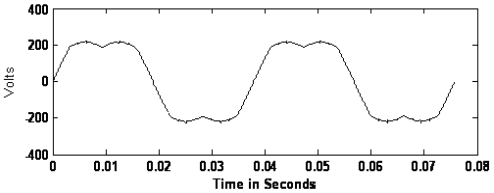

Fig. 11c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.42 (layer-5, 6-level operation)

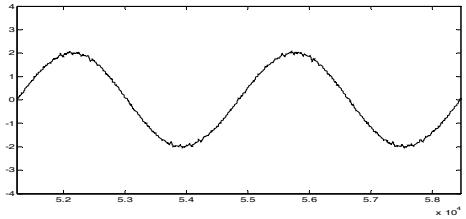

Fig. 11d. Motor phase current when M=0.42 (layer-5, 6-level operation)

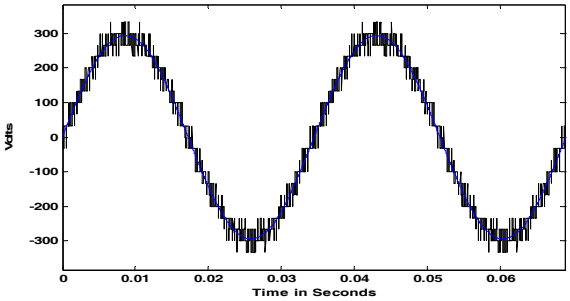

Fig. 12a. Motor phase voltage when M=0.5 (layer-6, 7-level operation)

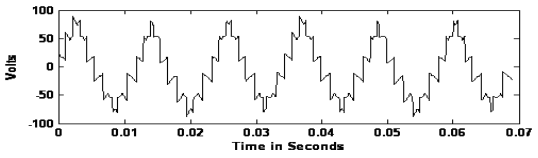

Fig. 12b. The offset voltage to be added to sinusoidal reference signals when M=0.5 (layer-6, 7-level operation)

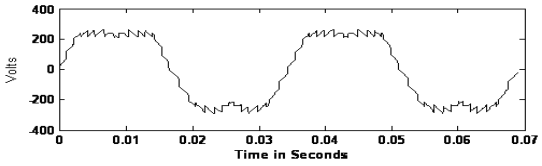

Fig. 12c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.5 (layer-6, 7-level operation)

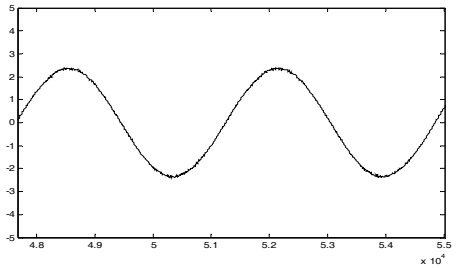

Fig. 12d. Motor phase current when M=0.5 (layer-6, 7-level operation)

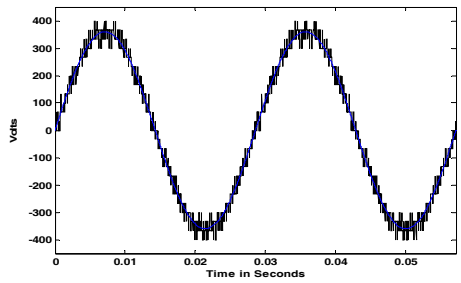

Fig. 13a. Motor phase voltage when M=0.6 (layer-7, 8-level operation)

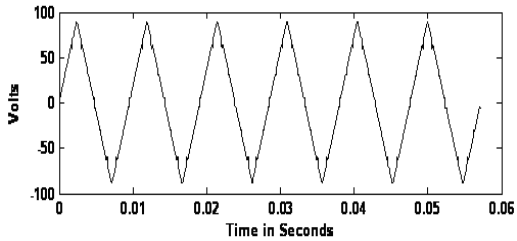

Fig. 13b. The offset voltage to be added to sinusoidal reference signals when M=0.6 (layer-7, 8-level operation)

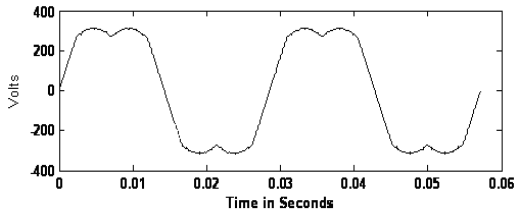

Fig. 13c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.6 (layer-7, 8-level operation)

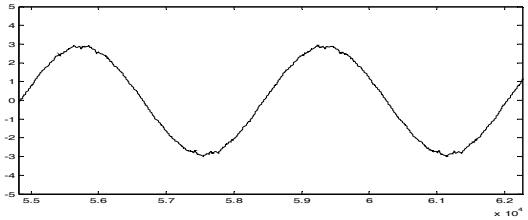

Fig. 13d. Motor phase current when M=0.6 (layer-7, 8-level operation)

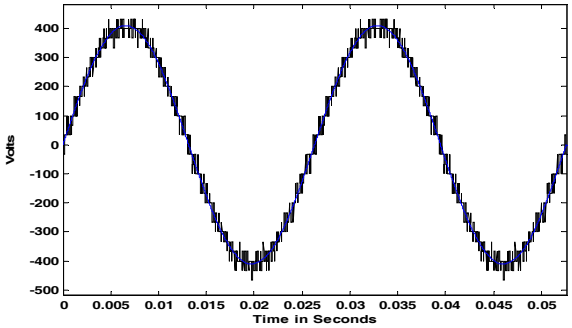

Fig. 14a. Motor phase voltage when M=0.65 (layer-8, 9-level operation)

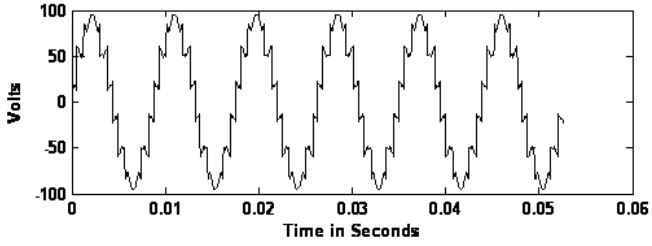

Fig. 14b. The offset voltage to be added to sinusoidal reference signals when M=0.65 (layer-8, 9-level operation)

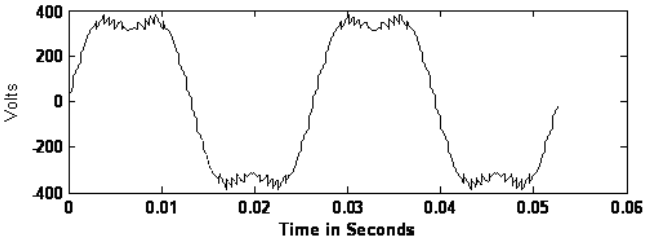

Fig. 14c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.65 (layer-8, 9-level operation)

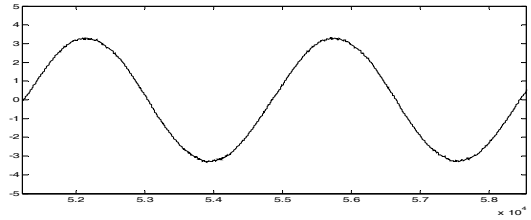

Fig. 14d. Motor phase current when M=0.65 (layer-8, 9-level operation)

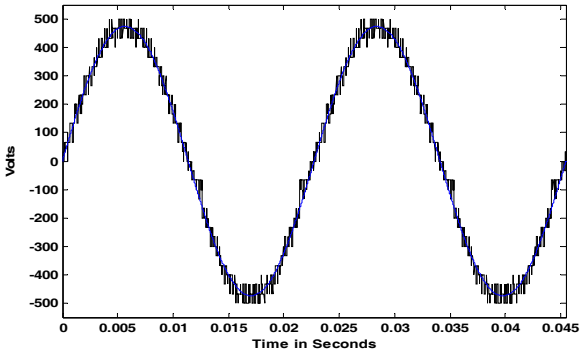

Fig. 15a. Motor phase voltage when M=0.75 (layer-9, 10-level operation)

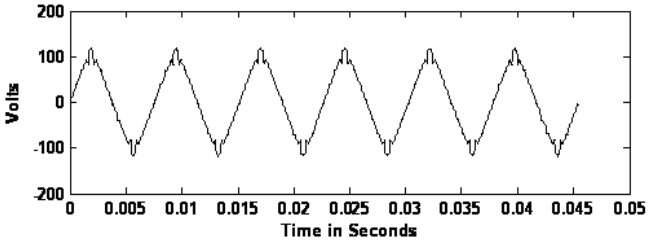

Fig. 15b. The offset voltage to be added to sinusoidal reference signals when M=0.75 (layer-9, 10-level operation)

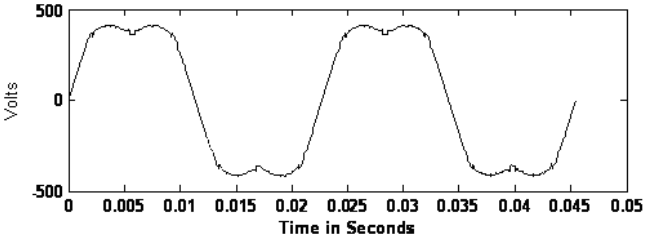

Fig. 15c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.75 (layer-9, 10-level operation)

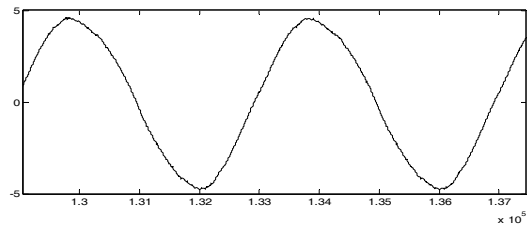

Fig. 15d. Motor phase current when M=0.75 (layer-9, 10-level operation)

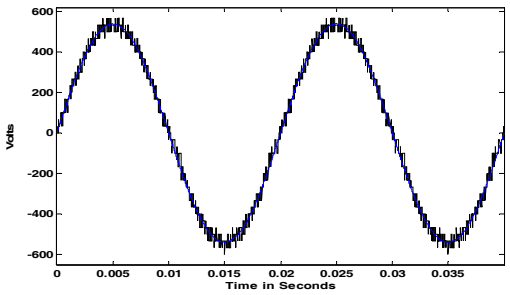

Fig. 16a. Motor phase voltage when M=0.85 (layer-10, 11-level operation)

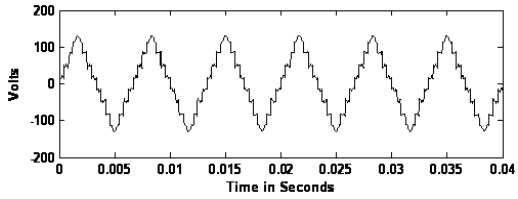

Fig. 16b. The offset voltage to be added to sinusoidal reference signals when M=0.85 (layer-10, 11-level operation)

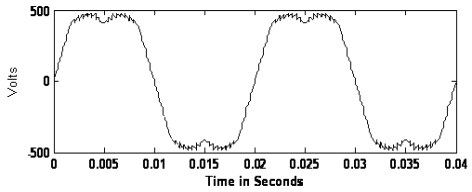

Fig. 16c. The A-phase sinusoidal reference signal after offset voltage is added when M=0.85 (layer-10, 11-level operation)

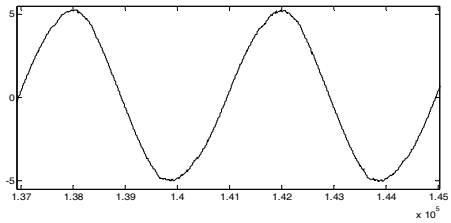

Fig. 16d. Motor phase current when M=0.85 (layer-10, 11-level operation)

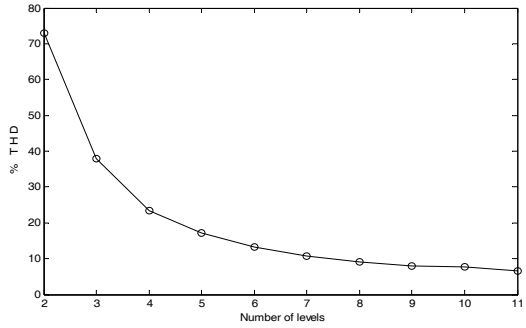

Fig. 17. Total harmonic distortion (%THD) as the number of levels increased

VIII. Conclusion

A modulation scheme of SVPWM for eleven-level inverter system for dual-fed induction motor drive, where the induction motor is fed by asymmetrical four-level inverter from one end and symmetrical three-level inverter from other end is presented. The asymmetrical four-level inverter used is composed of three conventional two-level inverters with unequal DC link voltage in cascade and the symmetrical three-level inverter used is composed of two conventional two-level inverters with equal DC link voltage in cascade. The centering of the middle inverter space vectors of the SVPWM is accomplished by the addition of an offset voltage signal to the sinusoidal reference signals, derived from the sampled amplitudes of the sinusoidal reference signals. The SVPWM technique, presented in this paper does not require any sector identification, as is required in conventional SVPWM schemes. The proposed scheme eliminates the use of look-up table approach to switch the appropriate space vector combination as in conventional SVPWM schemes. This reduces the computation time required to determine the switching times for inverter legs, making the algorithm suitable for real-time implementation.

References

[1] J. Holtz, "Pulse width modulation–A survey," *IEEE Trans. on Industrial Electronics*, vol.39, no.5, pp. 410–420., Dec. 1992.

[2] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEE Trans. on Industrial Electronics*, vol. 49, no. 1, pp. 186–196, Feb. 2002.

[3] H. W. Van Der Broeck, H. C. Skudelny, and G. V .Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Trans. on Industry* Applications, vol. 24, no. 1, pp. 142–150, Jan. /Feb. 1988.

[4] J. T. Boys and P. G. Handley, "Harmonic analysis of space vector modulated PWM waveforms," *IEE Proc. Electronic Power Applications,* vol. 137, no. 4, pp. 197–204., July 1990.

[5] V. T. Somasekhar and K. Gopakumar, "Three-level inverter Configuration cascading two 2-level inverters," *IEE Proc. Electronic Power Applications*, vol. 150, no. 3, pp. 245–254, May 2003.

[6] J. Holtz, W. Lotzkat, and A. M. Khambadkone, "On continuous control of PWM inverters in over-modulation range including six-step mode," *IEEE Trans. on Power Electronics*, vol. 8, no. 4, pp. 546–553., Oct. 1993.

[7] D. C. Lee and G. M. Lee, "A novel over-modulation technique for space vector PWM inverters," *IEEE Trans. on Power Electronics*, vol. 13, no. 6, pp. 1144–1151., Nov. 1998.

[8] J. Krah and J. Holtz, "High performance current regulation and efficient PWM Implementation for low inductance servo motors," *IEEE Trans. On Industry Applications,* vol. 35, no. 5, pp. 1039–1049, Sep. /Oct. 1999.

[9] D. G. Holmes, "The general relationship between regular sampled pulse width modulation and space vector modulation for hard switched converters," *Conf. Rec. IEEE Industry Applications Society (IAS) Annual Meeting*, Houston, 1992, pp. 1002–1009.

[10] J. Kim and S. Sul, "A novel voltage modulation technique of the Space Vector PWM," *Proc. Int. Power Electronics Conf., Yokohama, Japan,* 1995, pp. 742–747.

[11] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multi-level PWM method: A theoretical analysis," *IEEE Trans. on Power Electronics*, vol. 7, no. 3, pp. 497–505, July 1992.

[12] E. G. Shivakumar, K. Gopakumar, S. K. Sinha, P. Andre, and V. T. Ranganathan, "Space vector PWM control of dual inverter fed open-end winding induction motor drive," *Proc. Applied Power Electronics Conf. (APEC),* California, 2001, pp. 399–405.

[13] J. H. Suh, C. Choi, and D. Hyun, "A new simplified space vector PWM method for three-level inverter," *Proc. IEEE Applied Power Electronics Conf. (APEC),* Dallas, 1999, pp. 515–520.

[14] M. R. Baiju, K. K. Mohapatra, V. T. Somasekhar, K. Gopakumar, and L. Umanand, "A five-level inverter voltage space phasor generation for an open-end winding induction motor drive," *IEE Proc. Electronic Power Applications*, vol. 150, no. 5, pp. 531–538, Sep. 2003.

[15] F. Wang, "Sine-triangle versus space vector modulation for three level PWM voltage source inverters," *Proc. IEEE-IAS Annual Meeting,* Rome, 2000, pp. 2482–2488.

[16] M. R. Baiju, K. Gopakumar, V. T. Somasekhar, K. K. Mohapatra, and L. Umanand, "A space vector based PWM method using only the instantaneous amplitudes of reference phase voltages for three-level inverters," *EPEJ.*, vol. 13, no. 2, pp. 35–45, May 2003.

[17] B. P. McGrath, D. G. Holmes, and T. A. Lipo, "Optimized space vector switching sequences for multilevel inverters," *Proc. IEEE*

Applied Power Electronics Conf. (APEC), California, 2001, pp. 1123–1129.

[18] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, **"**Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *IEE Proc.-Electronic Power Applications,* vol. 152, no. 2, pp. 297-309, Mar. 2005.

[19] M. R. Baiju, K. Gopakumar, K. K. Mohapatra, V. T. Somasekhar, and L. Umanand, "Five-Level inverter voltage-space vector phasor generation for an Open-End Winding Induction Motor Drive,*" In: IEE proc.-power Applications,* vol. 150, no. 5, pp. 531-538, Sep. 2003.

G.Sambasiva Rao received B.E. degree in Electrical & Electronics Engineering from Andhra University Engineering College, Visakha Patnam, India in 2000 and M.E. with Power Electronics & Industrial Drives from Sathyabama Institute of Science and Technology, Chennai, India in 2006.

Since 2006, he has been with R.V.R & J.C.College of engineering as Lecturer. Presently he is a part-time research student at J.N.T.U College of Engineering, Hyderabad, India, working towards his doctoral degree.

Dr.K.Chandra Sekhar received his B.Tech degree in Electrical & Electronics Engineering from V.R.Siddartha Engineering College, Vijayawada, India in 1991 and M.Tech with Electrical Machines & Industrial Drives from Regional Engineering College, Warangal, India in 1994. He Received the PhD degree from the J.N.T.U College of Engineering, Hyderabad, India in 2008.

He is having 17 years of teaching experience. He is currently Professor and Head of Department, EEE, R.V.R & J.C.College of engineering, Guntur, India. His Research interests are Power Electronics, Industrial Drives & FACTS Devices.