Input DC Voltages of Three-level Neutral Point Clamped Voltage Source Inverter Balancing Using a New Kind of Clamping Bridge

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Abstract—A serious constraint in multilevel inverters is the capacitor voltage-balancing problem. The unbalance of the different DC voltage sources of the three-level Neutral Point Clamping Voltage Source Inverter (NPC-VSI) constituted the major limitation for the use of this power converter. To remedy to this problem, a new control solution to compensate the unbalanced DC voltages for the three-level NPC VSI is presented. It provides a fast and flexible control of the inverter capacitor voltages, leads to a simpler implementation, and present high equalization efficiency. Simulation results show the effectiveness of our methods.

Index Terms—Clamping bridge, Multilevel inverter, NPC VSI, Sliding mode control.

I. INTRODUCTION

One important problem associated with the NPC three-level inverter is its Neutral Point (NP) variation [1], the DC link NP potential can significantly fluctuate or continuously drift to unacceptable levels. The causes of NP potential drift can be non uniform switching device or DC link capacitor characteristics or fluctuation due to the irregular and unpredictable charging and discharging in each capacitor [2] [3] [4].

The voltage across the capacitor may grow or decay so that the NP voltage fails to keep the half of the DC link voltage. Therefore, an excessive high voltage may be applied to the switching devices of DC link capacitors and this affects the converter performance due to the generation of uncharacteristic harmonics and the presence of overvoltages across the semiconductor switches.

Therefore, the choice of appropriate modulation techniques and the development of advanced neutral point potential control techniques is necessary to overcome the NP potential problems.

Some solutions have been proposed, which are based on redundant switching configurations [1], [5]-[12] or on the addition of zero-sequence voltage components to the output voltage [6].

However, all these methods seem to be not always useful in no-load or low-load operations, when the supplied current tends to zero. In real systems, no-load conditions determine almost always the loss of DC-link capacitors voltages balance, owing to converter non ideality. Unfortunately, these methods modify the output voltage waveform. As the number of inverter-levels increases, the problem of capacitor balancing becomes more complex and the solution very drastic.

The unbalance DC voltage problem can also be solved by separate DC sources [3] or by adding electronic circuitry. In [13] and [14], clamping bridges based on transistors and resistors are proposed as a solution to this problem. Disadvantages of this method are the requirement for large power dissipating resistors, high current switches, and thermal management requirements. This method is best suited for systems that are charged often with small currents.

This paper deals introduces a new clamping bridge for the DC capacitor voltage equalisation has been proposed to compensate DC-link capacitors voltages fluctuations in a NPC VSI that permits to achieve a correct capacitors voltages sharing, when conventional balancing methods fail. The organization of this paper is as follows. Section 2 develops the mathematical modelling of the DC-AC converter (three-level NPC-VSI) and its Pulse Width Modulation control strategy (PWM) using two bipolar carriers. Section 3, provides the speed control of a Permanent Magnet Synchronous Machine based on sliding mode. The control of the three-level PWM current rectifier by sliding mode using feedback loops to regulate the average value of DC voltages and the network currents are discussed in section 4. Therefore, a clamping bridge control is introduced to improve the performance of voltage balance strategy in section 5. Finally, in the section 6, simulation will be implemented to present a study of the phenomenon, to demonstrate the proposed method and to report the effectiveness of this solution.

II. THREE-LEVEL CASCADE

We firstly propose a knowledge model of the three-phase three-level NPC-VSI inverter and develop a PWM strategy to control it (two bipolar carriers).

The global scheme of the cascade is given on the fig.1.

A. Three-level NPC-VSI modelling

The general structure of the three-phase three-level NPC
voltage source inverter is shown on the fig.2. It is composed by 12 pairs transistor-diode. Every leg of this inverter includes four pairs (two on the upper half leg and two on the lower one) and two diodes.

The optimal control law is given below:

\[ B_{k1} = B_{k4} \]
\[ B_{k2} = B_{k3} \]

\( B_{k} \) is the control signal of \( TD_{k} \). \( TD_{k} \) represent every pair transistor-diode by one bi-directional switch.

The voltage of the three phases A, B, C relatively to the middle point M and using the half leg connection functions \( F_{KM}^{b} \) are given by VXN with x = point A, B or C.

\[
\begin{align*}
V_{AM} &= F_{11}^{b} U_{c1} - F_{10}^{b} U_{c2} \\
V_{BM} &= F_{21}^{b} U_{c1} - F_{20}^{b} U_{c2} \\
V_{CM} &= F_{31}^{b} U_{c1} - F_{30}^{b} U_{c2}
\end{align*}
\]

\( V_{KM} \) are given by VXN with x = point A, B or C. The input currents of the three phases three-level inverter using the load currents are given by the following relations:

\[
\begin{align*}
I_{d1} &= i_{d1}^{b} + i_{d1}^{c} + i_{d1}^{b} + i_{d1}^{c} \\
I_{q2} &= i_{q2}^{b} + i_{q2}^{c} + i_{q2}^{b} + i_{q2}^{c} \\
I_{d0} &= i_{d0}^{b} + i_{d0}^{c} + i_{d0}^{b} + i_{d0}^{c}
\end{align*}
\]

### B. Control strategy of the inverter

This strategy uses two bipolar carriers (\( U_{p1} \), \( U_{p2} \)). It is characterised by two parameters \( m \) the index modulation and \( r \) the modulation rate. The algorithm of this strategy can be summarised as follows:

**Step 1:** Determination of the intermediate voltages

\[
\begin{align*}
\text{If } V_{refk} &\geq U_{p1} \Rightarrow V_{k1} = U_{c} \\
\text{If } V_{refk} &< U_{p1} \Rightarrow V_{k1} = 0 \\
\text{If } V_{refk} &\geq U_{p2} \Rightarrow V_{k0} = 0 \\
\text{If } V_{refk} &< U_{p2} \Rightarrow V_{k0} = -U_{c}
\end{align*}
\]

**Step 2:** Determination of the output voltage

\[ V_{KM} = V_{k1} + V_{k0} \]

### III. PERMANENT MAGNET SYNCHRONOUS MACHINE MODELLING

In this part, we present the PMSM modelling and its speed control by sliding mode.

The model of PMSM without damper winding has been developed on rotor reference frame as follows [13] [14] [15] [16]:

\[
\begin{align*}
V_{d} &= R_{s} i_{d} - p \Omega L_{q} i_{q} \\
V_{q} &= p \Omega L_{d} i_{d} + R_{s} i_{q} + \Omega \Phi_{f}
\end{align*}
\]

The electric torque is stated as:

\[ T_{e} = p \Phi_{f} i_{q} + (L_{d} - L_{q}) i_{d} i_{q} \]

Control of PM motors is performed using field oriented control for the operation of synchronous motor as a DC motor. For the PM synchronous machine used, we develop the algorithm \( i_{d} = 0 \) (Fig.3). When the \( d \) axis current is equal to zero, the block diagram of the \( q \) axis becomes similar to that of a DC machine and the speed can be controlled by using a sliding mode controller which generates the \( q \) axis voltage. We use a current regulator for the \( d \) and \( q \) axes [17] [18].

### IV. THREE-LEVEL PWM CURRENT RECTIFIER

The control of the three-level PWM current rectifier by sliding mode using feedback loops to regulate the average value of the two DC voltages and the network currents are
given.

The general structure of the three-level PWM current rectifier is given on the fig.4.

![Fig.4 Structure of the three-level PWM current rectifier](image)

A. Voltage feedback control

For each phase k (k=1, 2 or 3) of the three-phase network feeding, the rectifier considered can be represented by a R,L circuit. $V_{resk}$ is the voltage of one phase k of the three-phase network and $V_k$ is the voltage of the leg k of the rectifier.

The voltage loop imposes the effective value of the reference current of the network corresponding to the power exchanged between the network and the continue load (Fig.5).

![Fig.5 Control algorithm of the output DC voltage of the three-level PWM current rectifier](image)

For the voltage loop modelling, we use the instantaneous power conservation principle. In this principle, $P_{in}$ is the input power of the rectifier and $P_{out}$ the output one.

$$P_{in} = 3 \frac{V_{resk} \cdot I_{resk} - R \cdot I_{resk}^2 - L \cdot \frac{d}{dt} I_{resk}^2}{2}$$ (9)

$$P_{out} = U_{c1} \cdot (i_{ch1} + i_{cl}) + U_{c2} \cdot (i_{ch2} + i_{cl})$$ (10)

If we suppose the sinusoidal currents of the network in phase with the corresponding voltages $V_{resk}$ and we neglect the rectifier losses and the Joule effect in the network resistors R, we can write:

$$P = 3V_r \cdot I_e = 2U_c \cdot I_{red}$$ (11)

Then

$$I_{red} = \frac{3V_r \cdot I_e}{2U_c}$$ (12)

We define the next values as follows:

$$U_c = \frac{U_{c1} + U_{c2}}{2}$$

$$i_c = \frac{i_{cl} + i_{c2}}{2}$$ (13)

$$i_{ch} = \frac{i_{ch1} + i_{ch2}}{2}$$

$$I_{red} = i_{ch} + i_c$$

We want to regulate the voltage $U_c$ of the rectifier. For that, we choose for sliding surface:

$$S = U_c - U_{cref}$$ (14)

Its derivative is:

$$\dot{S} = U_c$$ (15)

$$\dot{U}_c = \frac{(I_{red} - i_{ch})}{C}$$ (16)

If we replace (12) in (16), we obtain:

$$\dot{U}_c = \frac{3V_r \cdot I_e}{2U_c} - i_{ch}$$ (17)

The condition $\dot{S} < 0$ insures the attractibility of the trajectory towards the sliding surface. For that, we choose:

$$\dot{S} = -k_1 \cdot \text{sign}(S) - k_2 \cdot S$$ (18)

The output of the sliding mode controller gave:

$$I_e = -[C \cdot (k_1 \cdot \text{sign}(U_c - U_{cref}) + k_2 \cdot (U_c - U_{cref}) - i_{ch}) \cdot \frac{2U_c}{3V_r}]$$ (19)

B. Current feedback control

We control the network current of the phase 1 and 2 by a sliding mode regulator. The algorithm of this current loop is given on the fig.6. In this scheme, the transfer function $H(s)$ is expressed as follows:

$$H(s) = \frac{I_{resk}}{V} = \frac{1}{R + L \cdot s}$$ (20)

![Fig.6 Control algorithm of the network current $i_{resk}$ of the three-level PWM rectifier](image)

From the network equations we have:
\begin{align}
V_{\text{ref}} - V_A &= R \dot{I}_{\text{ref}} + L \ddot{I}_{\text{ref}} \\
V_{\text{ref}} - V_B &= R \dot{I}_{\text{ref}} + L \ddot{I}_{\text{ref}}
\end{align}
\tag{21}
\begin{align}
\dot{V}_A &= N_{g1} U_c \\
\dot{V}_B &= N_{g2} U_c
\end{align}
\tag{22}

We choose the following sliding surfaces
\begin{align}
\dot{S}_1 &= I_{\text{ref}} - I_{\text{ref}} \\
\dot{S}_2 &= I_{\text{ref}} - I_{\text{ref}}
\end{align}
\tag{23}

To satisfy the attractibility condition, we choose:
\begin{align}
\dot{S}_1 &= -k_{11} \text{sign}(S_1) - k_{21} S_1 \\
\dot{S}_2 &= -k_{12} \text{sign}(S_2) - k_{22} S_2
\end{align}
\tag{24}
\begin{align}
\dot{S}_k &= I_{\text{ref}} - \sqrt{2} \omega L e \cos(\omega t - 2(k-1)\pi/3)
\end{align}
\tag{25}

with \( k = 1, 2, 3 \)

We obtain:
\begin{align}
N_{g1} &= [V_{\text{ref}} - R I_{\text{ref}} + L k_{11} \text{sign}(I_{\text{ref}} - I_{\text{ref}}) + L k_{21} (I_{\text{ref}} - I_{\text{ref}}) - \sqrt{2} L \omega L e \cos(\omega t)]/2U_c \\
N_{g2} &= [V_{\text{ref}} - R I_{\text{ref}} + L k_{12} \text{sign}(I_{\text{ref}} - I_{\text{ref}}) + L k_{22} (I_{\text{ref}} - I_{\text{ref}}) - \sqrt{2} L \omega L e \cos(\omega t - 2\pi/3)]/2U_c
\end{align}
\tag{26}

V. CLAMPING BRIDGE

In this section, a clamping bridge control is introduced to balance the two DC input voltages, avoid NP potential drift and improve the performances of the speed control of the permanent magnet synchronous machine.

Several publications have discussed ways to solve this balancing problem in three-level NPC-VSI [5-14]. The multitude of proposals (selection of appropriate voltage vectors) implemented to ensure DC voltage balancing can be broadly divided into two categories. In the first category based on space vector realization, redundant switching states of the converter are used while in the second category using carrier-based pulse width modulation (PWM) scheme, a zero sequence voltage signal is added to the modulation signals. In some schemes using zero sequence voltage to balance DC capacitor voltages, knowledge of load power factor (or direction of instantaneous power flow) is required which is difficult to implement under transient conditions, and in others, measurements of both capacitor voltages and load currents (magnitudes or polarities) are required. Unfortunately, these methods modify the output voltage waveform. Also, as the number of inverter-levels increases, the problem of capacitor balancing becomes more complex and the solution very drastic.

By using a separate supply for each DC-link level, the balancing issues are solved [3]. However, this solution is expensive especially for more than three-level. Another solution consists of adding electronic circuitry. In [13] and [14], clamping bridges based on transistors and resistors are proposed as a solution to this problem.

Advantages are low cost and low complexity. Disadvantages are high energy losses, high current switches and costly design thermal management requirements for large values. This method is best suited for systems that are charged often with small currents.

In order to remedy to the unbalance problem, we suggest a solution which consists in establish a bridge balancing between the rectifier and the intermediate filter (fig.7). The aim of this use is to limit and stabilise variations of the input DC voltages of the inverter.

The capacitor voltage equalization clamping bridge scheme has many advantages such as higher equalization efficiency and a modular design approach.

The balancing algorithms search to efficiently remove energy from a strong capacitor and transfer that energy into a weak one until the capacitor voltage is equalized across all capacitors.

Every switch \( T_x \) \( (x=1,2,3,4) \) represent a pair transistor-diode.

A. Switch control strategy of the clamping bridge

Step 1: Deduction of the sign of the differences. We use the following equations:
\begin{align}
C. \frac{d(U_{c1} - U_{c2})}{dt} &= (i_{L1} + i_{L2} + i_{d0} - i_{c1})
\end{align}
\tag{27}

Step 2: Deduction of the command of the transistors
\begin{align}
U_{c2} > U_{c1} \Rightarrow T_2 = 1; T_1 = 0 \\
U_{c1} > U_{c2} \Rightarrow T_2 = 0; T_1 = 1
\end{align}
\tag{28}

VI. SIMULATION RESULTS

In order to validate the solution proposed previously, we present simulation results for the three-level PWM current rectifier – three-level NPC-VSI – PMSM cascade. In the first case, the clamping bridge will not be used in order to show the instability problem of the two input DC voltages.
In the second one, the solution proposed is introduced to improve the performances of DC voltages and PMSM.
Fig. 15: Voltage $U_{c2}$

Fig. 16: Speed and its reference

Fig. 17: Electromagnetic torque

Fig. 18: $d$ axis current ($i_d$)

Fig. 19: $q$ axis current ($i_q$)

Fig. 20: Voltages $U_{c1}$ and $U_{c2}$

Fig. 21: Speed and its reference

Fig. 22: Electromagnetic torque
VII. RESULTS AND DISCUSSIONS

Figure 8 shows the reference voltages and the two carriers used for this strategy. We can see on this figure that the voltage $V_{AM}$ has three levels (fig.9). Fig.10 shows the output voltage $V_A$ and its harmonic spectrum for $m=12$ (fig.11). We notice that the harmonics gather by families centred around frequencies multiple of 2.m.f.

Fig.12 shows the voltage $U_c$ and its reference obtained by controlling the three-level PWM rectifier controlled by sliding mode. This voltage follows perfectly its reference (200V). The network current $i_{res1}$ is in phase with the network voltage $V_{res1}$ (fig.13).

We show perfectly the problem of the unbalance of the two DC voltages of the intermediate capacitors bridge. The voltage $U_{c1}$ (fig.14) is increasing and the voltage $U_{c2}$ (fig.15) is decreasing.

The characteristics of the drive of the PM synchronous machine (Speed (fig.16), torque (fig.17) and different currents (fig.18 and fig.19)) fed by a three-level PWM current rectifier – three-level NPC VSI cascade show that the undulations of the currents $i_d$, $i_q$ and the electromagnetic torque are very important.

These results show the importance of the stability of the input DC voltages of the inverter to have good performances for the speed control of the PM synchronous machine.

Fig.20 to 24 show the different input DC voltages obtained by using the stabilisation bridge. We can see that the output voltages of the rectifier ($U_{c1}$ and $U_{c2}$ (fig.20)) stabilise around 200V. By using this technique of stabilisation, we can remark that the undulations on the performances (Speed (fig.21), Torque (fig.22) and currents $i_d$ (fig.23) and $i_q$ (fig.24)) of the PMSM disappear and those performances are improved by using the Clamping bridge.

VIII. CONCLUSION

The present contribution intends to demonstrate that permanent magnet synchronous machine control based on sliding mode control when applied with a three-level PWM current rectifier – Three-level PWM NPC-VSI may contribute both for functional performances improvement and attenuation of some technological limitations. With a high number of semi-conducting devices, current and voltage quality are improved and weight reduced by avoiding heavy filters.

The input DC voltages are generated by a three-level PWM current rectifier controlled by sliding mode control. By this study, we have particularly shown the problem of the stability and its effects on the speed control of PMSM and the input DC voltages sources of the inverter.

In the last part of this paper, we propose a simple solution to stabilise the two DC voltages by using a clamping bridge composed by two switches (pair transistor-diode) and one inductance.

This technique permit an economic and simple electronic implementation, whereas in the space vector modulation control the computational burden, the complexity of the algorithms and the number of instructions are drastic especially when the number of levels of the inverter is greater than three.

APPENDIX

$B_{ks}$ : Control signal of $TD_{ks}$

$TD_{ks}$ : Pair transistor-diode

$F_{kt}$ : Connection function of a half arm

$U_{p1}$, $U_{p2}$ : The two bipolar carriers

$V_{ref1}$, $V_{ref2}$, $V_{ref3}$ : The three reference voltages

$m$ : Index modulation

$r$ : Modulation rate

$L_d$, $L_q$ : self inductance of the d and q armatures equivalent winding.

$R_s$ : resistance of an armature winding.

$\omega$ : angular speed.

$s$ : Laplace operator.

$J$ : inertia of the set machine-load

$C_p$ : Load torque.

$e_d$ : Error variable

$S_d$ : Surface variable

$V_{resk}$ : Network voltage of one phase $k$

$V_k$ : Voltage of the leg $k$ of the rectifier.

$R$ : Network resistance

$L$ : Network inductance

* The parameters of the PM synchronous machine are:

$L_d=L_q=3.2$ mH ; $R_s=1$Ω ; $p=3$ ; $\Phi_f=0.13$N.m/A ;

$J=6.10^{-4}$ kg.m² ; $F_c=9,5. 10^{-5}$ N.m.s/rad
The parameters of the capacitors are: $C_1 = C_2 = 20 \text{mF}$

The parameters of the Clamping bridge are: $L_1 = 1 \text{mH}$

The parameters of the net are: $R = 0.25 \Omega$; $L = 10 \text{mH}$

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