Additional realizations of single-element-controlled oscillators using single ICCII-

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Abstract— **This paper presents additional realizations of single-element-controlled oscillators (SECOs) using a single negative-type inverting second-generation current conveyor (ICCII-). The circuits have been derived from a single ICCII-based topology previously proposed by Toker et al. Both single-resistance-controlled oscillators (SRCOs) and SECOs have been obtained. The circuits use one ICCII- and five/six external passive components, hence reduced number of components are employed. The circuits also provide explicit-current-output (ECO) and enjoy low active and passive sensitivities. PSPICE experimental results have been included to verify the theoretical results.**

Index Terms— **Active RC circuits, Single-element-controlled oscillators (SECOs), inverting second-generation current conveyor (ICCII)**

I. INTRODUCTION

Sinusoidal oscillators find numerous applications in communication, control systems, signal processing, instrumentation and measurement systems and the applications and advantages in realizing RC sinusoidal oscillators using second generation current conveyors (CCIIs) have received considerable attention [1]-[7] in the past. In 1999, Awad and Soliman introduced a new active building block (ABB), namely the inverting second generation current conveyor (ICCII) and which is an additional block to the current conveyor family [8]. This ABB besides possessing the advantages of its predecessor (CCII) had additional advantageous features of obtaining current-mode circuits from their voltage-mode counterparts by using the ad joint network theorem [9] as explained in [8]. Several circuit solutions using ICCII have been reported in the literature [10]-[12]. The aim of this brief is to present new single-resistance-controlled oscillators (SRCOs) and single-element-controlled oscillators (SECOs) using this versatile ABB. SRCOs provide independent control of condition of oscillation (CO) and frequency of oscillation (FO) by means of different resistors and SECOs provide single-element-control of oscillation frequency by either a resistor or a capacitor. The proposed oscillators are additions to the previously reported circuits in [13], which are categorized according to the number of ABBs used. But

most of the SRCOs or SECOs presented in [13] make use of multiple ABBs. One single ICCII based SRCO is also provided in [10] (see Fig. 3, topology 2 of [13]), but a detailed analysis of the proposed topology indicates that more SRCOs/SECOs could be derived from the same structure and hence the motivation is to come up with more oscillator circuits having single-element-control over condition of oscillation and frequency of oscillation, from the existing single negative type ICCII (ICCII-) based topology in [13]. Total of six oscillator circuits are reported in this brief, which include both SRCOs and SECOs. The oscillator circuits use reduced number (five/six) of external passive components (only resistors and capacitors). The circuits are also capable of providing explicit-current-output (ECO) by use of a dual-output ICCII and they could be used as current-mode oscillators in various current-mode signal processing applications. Numerous applications of the proposed circuits have been provided and the non-ideal analysis and sensitivity study have been carried out. PSPICE simulations have been included which verify the workability of the circuits.

II. INVERTING SECOND-GENERATION CURRENT CONVEYOR (ICCII)

The ICCII was first introduced in [8] and in this brief its variant, namely the dual-output negative type ICCII i.e. DOICCII- is used which is characterized by the following

$$\begin{pmatrix} I_y \\ V_x \\ I_{z+}, I_{z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix} \quad (1)$$

The circuit symbol of dual-output ICCII- is shown in Fig. 1 and the CMOS implementation could be found in [8], [12] and [13].

III. PROPOSED CONFIGURATION

The single ICCII- based topology is shown in Fig. 2. It is a general structure and various oscillator circuits can be derived out of it by appropriately choosing the admittances. As pointed in [13], this topology is meaningful only with ICCII but not with CCII since the admittance between *y* and *x* terminals of the conveyor is redundant for the latter. The possible SRCOs and SECOs have been attempted in this paper. The characteristic equation for the circuit shown in Fig. 2, in terms of the admittances can be found as

$$y_1 y_3 + y_5(y_1 + y_3 + 2y_2) = y_1 y_4$$

(2)

The various SRCOs and SECOs derived from this topology by choosing different combinations of passive components (the resistors and capacitors), along with the condition of oscillation (CO) and frequency of oscillation have been tabulated in Table I. From Fig. 2, it is clear that all the oscillators provide an explicit-current-output (ECO) by means of a duplicate current terminal z_2 (high output impedance terminal). This classifies the circuit as a current-mode oscillator and makes it suitable to be used in various current-mode signal processing applications [14]. As an example, these circuits could be used as sinusoidal input current-sources for current-mode active filters.
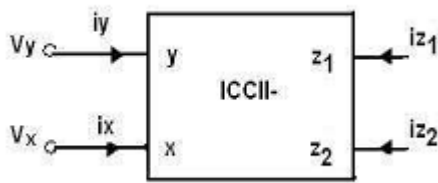

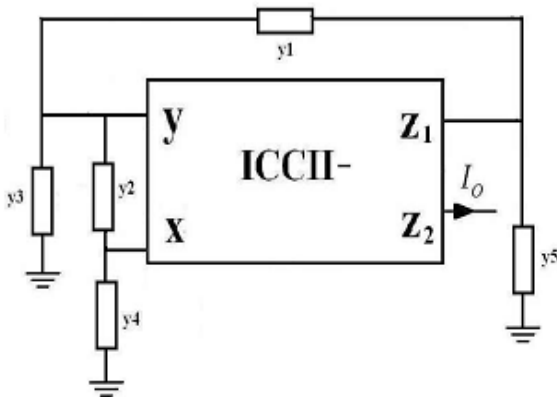Fig. 1: Symbolic Representation of dual-output ICCII-

Fig. 2: Proposed single ICCII- based oscillator topology

Although CO and FO control by means of resistors is more easy and preferable, but as pointed in [15], circuits with CO or FO control by means of capacitors are not out-classed when considered from the perspective of instrumentation and measurement applications, as single-element-control of FO through a capacitor can be used as transducer oscillators in conjunction with capacitive transducers, those providing CO control through a capacitor can be used in some capacitance measurement schemes such as mentioned in [15]-[16] and references provided therein. The circuit number 1 (see Table 1) is a true SRCO with CO and FO controls by means of different resistors. This circuit is the same as that proposed in (Fig. 3, topology 2) [13]. For the circuit number 2, the CO and FO tuning laws indicate that it is a SECO with single-element-control of the oscillation frequency by means of R_2. This oscillator has another unique application: since the numerator of FO has a difference term, the circuit could be used as a very low

frequency oscillator (VLFO) [17]. The circuit number 3 works as a SECO under the appropriate matching constraints, but it uses grounded capacitors which makes it suitable for monolithic integration [12] and [18]. Both circuit number 2 and 3 could be easily modified to create voltage-controlled oscillators (VCOs), by replacing resistor R_4 and R_3 respectively with a non-linearity cancelled MOSFET (working in triode-region) [19]-[20]. VCOs have wide applications, example in phase-locked loop (PLL), A/D convertors etc. as pointed in [15]. Additional oscillator circuits could be created from the circuits 1, 2 and 3 by simple applying the RC-CR transformation, i.e. replacing capacitors by resistors and vice-versa. This would lead to three new SECOs, all of which would have FO control by means of a capacitor. Hence a total of six new oscillator circuits have been derived from a single ICCII- based configuration.

IV. NON-IDEAL ANALYSIS AND SENSITIVITY STUDY

Considering the non-idealities of ICCII- as pointed in [8] and

[13], then $V_x = -aV_y$, $I_{z1} = -bI_x$ where α and β differ from their ideal values of unity of voltage-tracking and current-tracking errors respectively. Taking into account the above non-ideal effects, the basic characteristic equation of the oscillator topology as in (2) gets modified to

$$y_1 y_3 + y_5(y_1 + y_3 + (1+a)y_2) =$$

$$aby_1 y_4 + (1+a)(b-1)y_1 y_2 \qquad (3)$$

Both the CO and FO corresponding to every circuit get modified in the non-ideal case and could be easily derived using (3), the final results of which have been provided in Table II. It is evident from Table II, that only the FO of circuit number 3 remains unaffected from the non-idealities. Also, the sensitivity study indicates that the circuits enjoy low (less than unity) f_o active and passive sensitivities (see Table III). The non-ideal analysis and sensitivity study of the three additional SECOs created by RC-CR transformation from circuits 1, 2 and 3, could be carried out in a similar manner.

V. SIMULATION RESULTS

The working of all the proposed circuits as sinusoidal oscillators has been verified by PSPICE simulations. The circuit number 1, the SRCO employing five passive components is chosen as a design example. The simulations have been performed using a CMOS realization of ICCII- as provided in [12] and the parameters like the aspect ratio, biasing current and supply voltages were also chosen as in [12]. The circuit has been designed with the following passive component values: $C_1 = C_3 = 1nF$ and $R_2=R_4=1K\Omega$, $R_5= 2K\Omega$. With these component values the CO is satisfied and theoretical frequency of oscillation is *159.1 KHz*. The typical waveform of the voltage at terminal z_1 depicting the steady-state sinusoidal oscillations is shown in Fig. 3. As pointed earlier the circuit no. 1 is SRCO with FO control by means of G_2; the variation of the FO with resistor R_2 is shown in Fig. 4 and simulated values have close
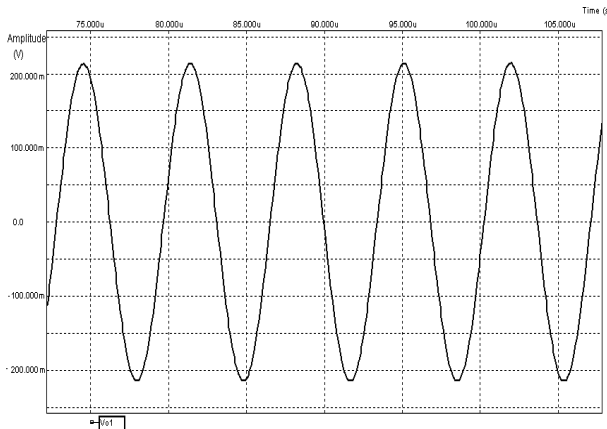
correspondence with theoretical values.
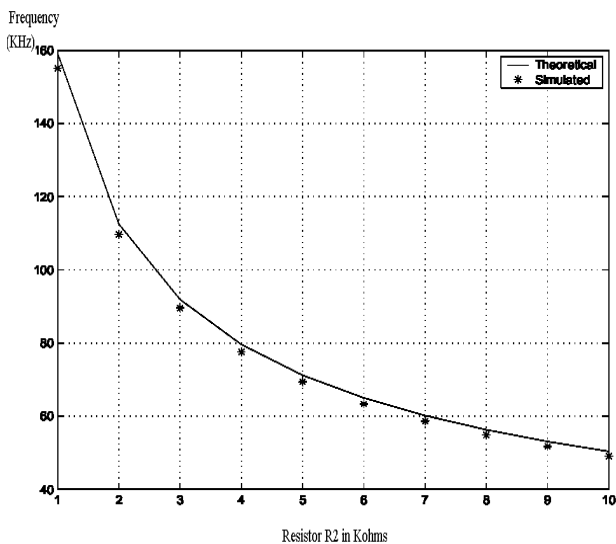

Fig.3 Steady-state time domain waveform

Fig. 4 Variation of FO with R2

VI. Conclusions

New single-element-controlled oscillator circuits have been devised from a previously proposed single negative type inverting current conveyor (ICCII-) based topology. The circuits enjoy single-element-control of oscillation of frequency and are suitable to be used as variable frequency oscillators. Oscillator circuits with advantageous features to be used as very-low frequency oscillators and/or voltage-controlled oscillators have also been created. All the circuits provide an explicit-current-output which could be used as an input/test sinusoidal signal in many current-mode circuits, particularly in current-mode filters. The circuits also exhibit low active and passive f_o sensitivities. PSPICE simulations have verified the workability of the circuits. The circuits add to the current repertoire of ICCII based oscillators circuits and the author is currently working on creating canonic oscillator structures using ICCII and two grounded capacitors- which shall be reported soon.

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Table I: CO and the FO comparisons of the proposed oscillators

Circuit	y_1	y_2	y_3	y_4	y_5	CO	FO (f_o)	Control of CO	Control of FO
1.	sC_1	G_2	sC_3	G_4	G_5	$G_4 = (1 + \frac{C_3}{C_1})G_5$	$\frac{1}{2\pi}\sqrt{\frac{2G_2G_5}{C_1C_3}}$	G_4	G_2
2.	G_1	sC_2	0	$sC_4 + G_4$	$sC_5 + G_5$	$2C_2G_5 = (C_4 - C_5)G_1$	$\frac{1}{2\pi}\sqrt{\frac{G_1(G_5-G_4)}{2C_2C_5}}$	C_4	G_4
3.	G_1	0	$G_3 + sC_3$	sC_4	sC_5	$C_5G_3 + C_5G_1 + C_3G_1 = C_4G_1$	$\frac{1}{2\pi}\sqrt{\frac{G_1G_3}{C_3C_5}}$	If $G_1 = G_3$, then by C_4	G_1, G_3

Table II: Modified CO and FO for the non-ideal case

Circuit	CO	FO (f_o)
1.	$C_1G_2(1 + \alpha)(\beta - 1) + \alpha\beta C_1G_4 = G_5(C_3 + C_1)$	$\frac{1}{2\pi}\sqrt{\frac{(1+\alpha)G_2G_5}{C_1C_3}}$
2.	$(1 + \alpha)C_2G_5 = (\alpha\beta C_4 - C_5)G_1 + (1 + \alpha)(\beta - 1)C_2G_1$	$\frac{1}{2\pi}\sqrt{\frac{G_1(G_5-\alpha\beta G_4)}{(1+\alpha)C_2C_5}}$
3.	$C_5G_3 + C_5G_1 + C_3G_1 = \alpha\beta C_4G_1$	$\frac{1}{2\pi}\sqrt{\frac{G_1G_3}{C_3C_5}}$

Table III: fo active and passive sensitivities

Circuit	f_o Sensitivities
1.	$\left|S^{f_o}_{C_1,C_3,G_2,G_5}\right| = \frac{1}{2}$,
	$S^{f_o}_{\alpha} = \frac{\alpha}{2(1+\alpha)}$,
	$S^{f_o}_{\beta} = 0$
2.	$\left|S^{f_o}_{C_2,C_5,G_1}\right| = \frac{1}{2}$,
	$S^{f_o}_{G_5} = \frac{G_5}{2(G_5-\alpha\beta G_4)}$,
	$S^{f_o}_{G_4,\beta} = \frac{-\alpha\beta G_4}{2(G_5-\alpha\beta G_4)}$,
	$S^{f_o}_{\alpha} = \frac{-\alpha\beta G_4}{2(G_5-\alpha\beta G_4)} - \frac{\alpha}{2(1+\alpha)}$
3.	$\left|S^{f_o}_{C_3,C_5}\right| = \frac{1}{2}$,
	If $G_1 = G_3$, $S^{f_o}_{G_1,G_3} = 1$,
	$S^{f_o}_{\alpha,\beta} = 0$

Abhirup Lahiri is currently with the Digital Processing Group, Division of Electronics and Communications, Netaji Subhas Institute of Technology, University of Delhi. His research interests include mixed-mode circuit design, analog signal processing and noise analysis of circuits. He has authored and co-authored twenty international journal, conference papers and design ideas and has acted as a reviewer (by editor's invitation) for international journals. He is a member of IACSIT, IAENG and ACEEE